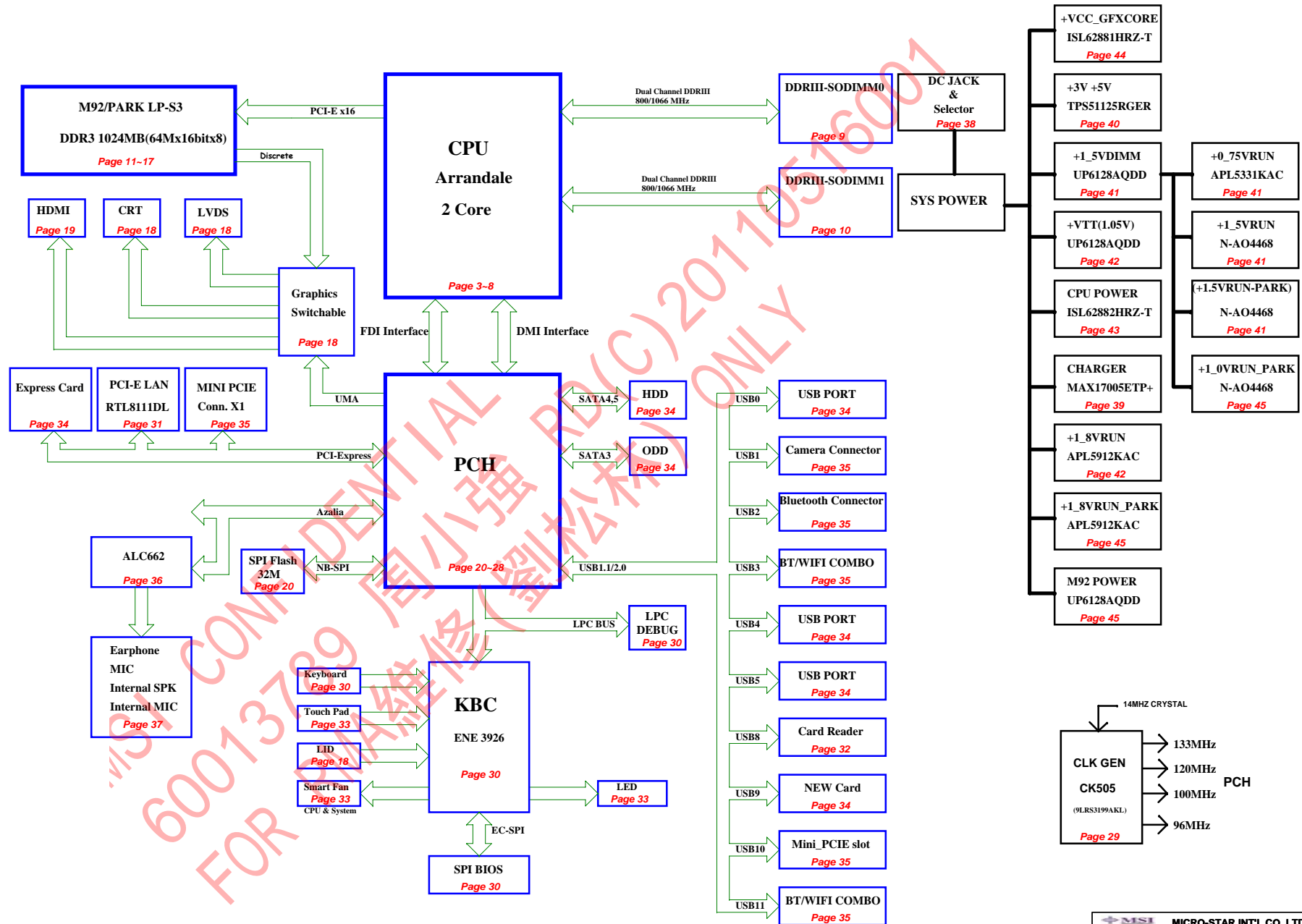


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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

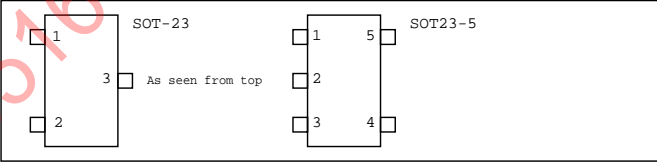
Voltage Rails

| POWER PLANE | VOLTAGE | ACTIVE IN | DESCRIPTION |
|---------------|------------|------------|--|
| PWR_SRC | 19V | S0,(S3-S5) | LAN DDRIII core PCH DDRIII command & control pull up. CPU core rail Graphics core rail (Dual Core only) |
| +5VALW | 5V | S0,(S3-S5) | |
| +5VRUN | 5V | S0 | |
| +5VSUS | 5V | S0 | |
| +3VALW | 3.3V | S0,(S3-S5) | |
| +3VSUS | 3.3V | S0,(S3-S5) | |
| +3VRUN | 3.3V | S0 | |
| +1_5VDIMM | 1.5V | S0,S3 | |
| +1_5VRUN | 1.5V | S0 | |
| VTT | 1.05V | S0 | |
| +0_75VRUN | 0.75V | S0 | |
| +VCC_CORE | 1.05V-1.1V | S0 | |
| +VCC_GFXCORE | 1.1V | S0 | |
| M92S_VDD_CORE | 0.95V | S0 | GPU core power GPU PCIE power GPU DDR3 power GPU PCIE power GPU I/O and DAC power |
| +1_8VRUN_PARK | 1.8V | S0 | |
| +1_5VRUN_PARK | 1.5V | S0 | |
| +1_0VRUN_PARK | 1.0V | S0 | |
| VDDR3 | 3.3V | S0 | |

Net Naming Conventions

| |
|--|
| Suffix |
| # = Active Low Signal |
| Prefix |
| H = Host |
| M = DDR Memory |
| TP = Test Point (does not connect anywhere else) |

PCB Footprints



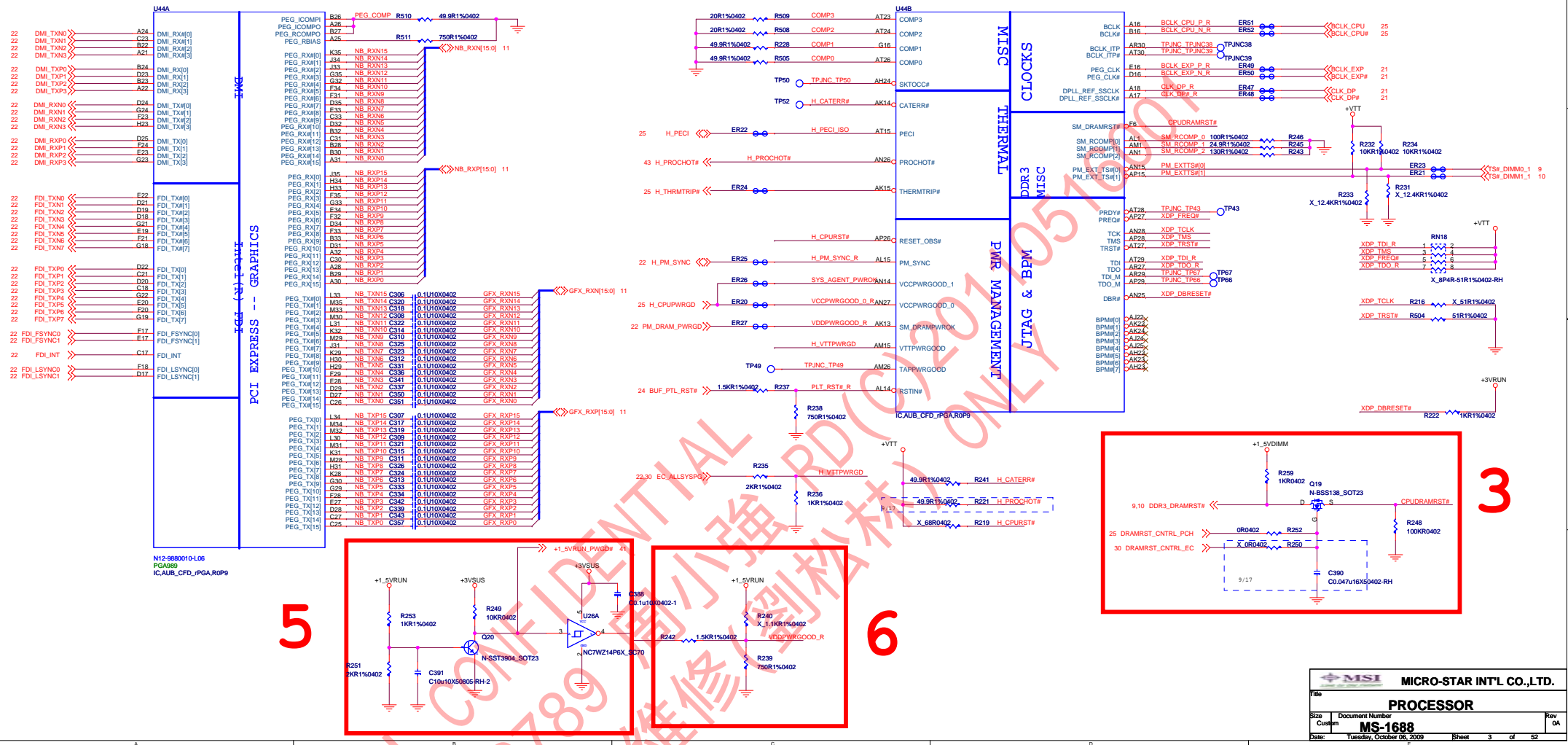
AC Mode

| Power States | SLP_S3# | SLP_S4# | SLP_S5# | SLP_LAN# | +V*ALWAYS | +V*SUS | +V*RUN | CLK |
|----------------------|---------|---------|---------|----------|-----------|--------|--------|-----|
| S0 (Full on) | HIGH | HIGH | HIGH | HIGH | ON | ON | ON | ON |
| S3 (Suspend to RAM) | LOW | HIGH | HIGH | HIGH | ON | ON | OFF | OFF |
| S4 (Suspend to Disk) | LOW | LOW | HIGH | HIGH | ON | ON | OFF | OFF |
| S5 (Soft Off) | LOW | LOW | LOW | HIGH | ON | ON | OFF | OFF |

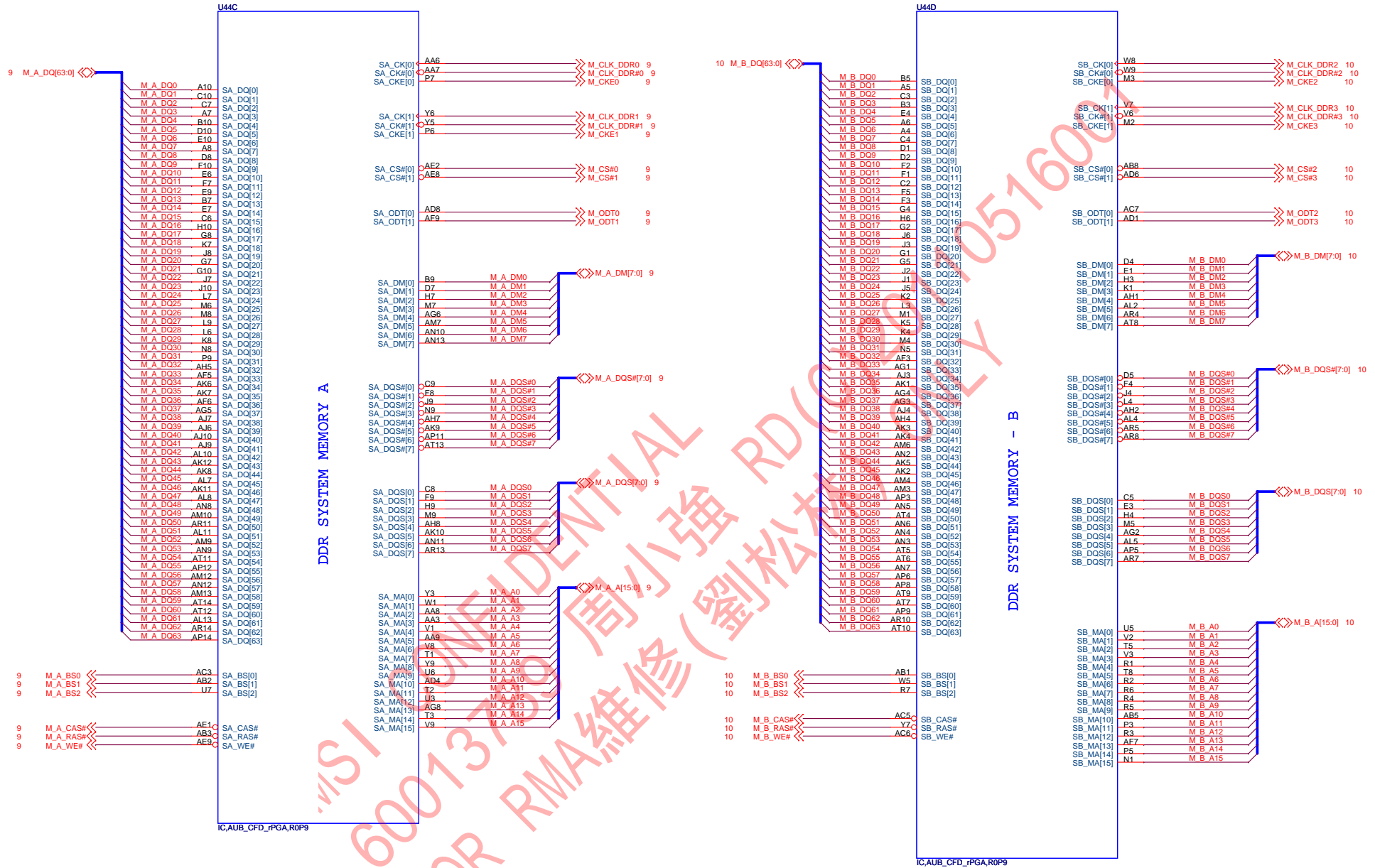
Battery Mode

| Power States | SLP_S3# | SLP_S4# | SLP_S5# | SLP_LAN# | +V*ALWAYS | +V*SUS | +V*RUIN | CLK |
|----------------------|---------|---------|---------|----------|-----------|--------|---------|-----|
| S0 (Full on) | HIGH | HIGH | HIGH | HIGH | ON | ON | ON | ON |
| S3 (Suspend to RAM) | LOW | HIGH | HIGH | HIGH | ON | ON | OFF | OFF |
| S4 (Suspend to Disk) | LOW | LOW | HIGH | HIGH | ON | OFF | OFF | OFF |
| S5 (Soft Off) | LOW | LOW | LOW | HIGH | ON | OFF | OFF | OFF |

ARRANDALE PROCESSOR (CLK,MISC,JTAG)



ARRANDALE PROCESSOR (DDR3)



ARRANDALE PROCESSOR (POWER)

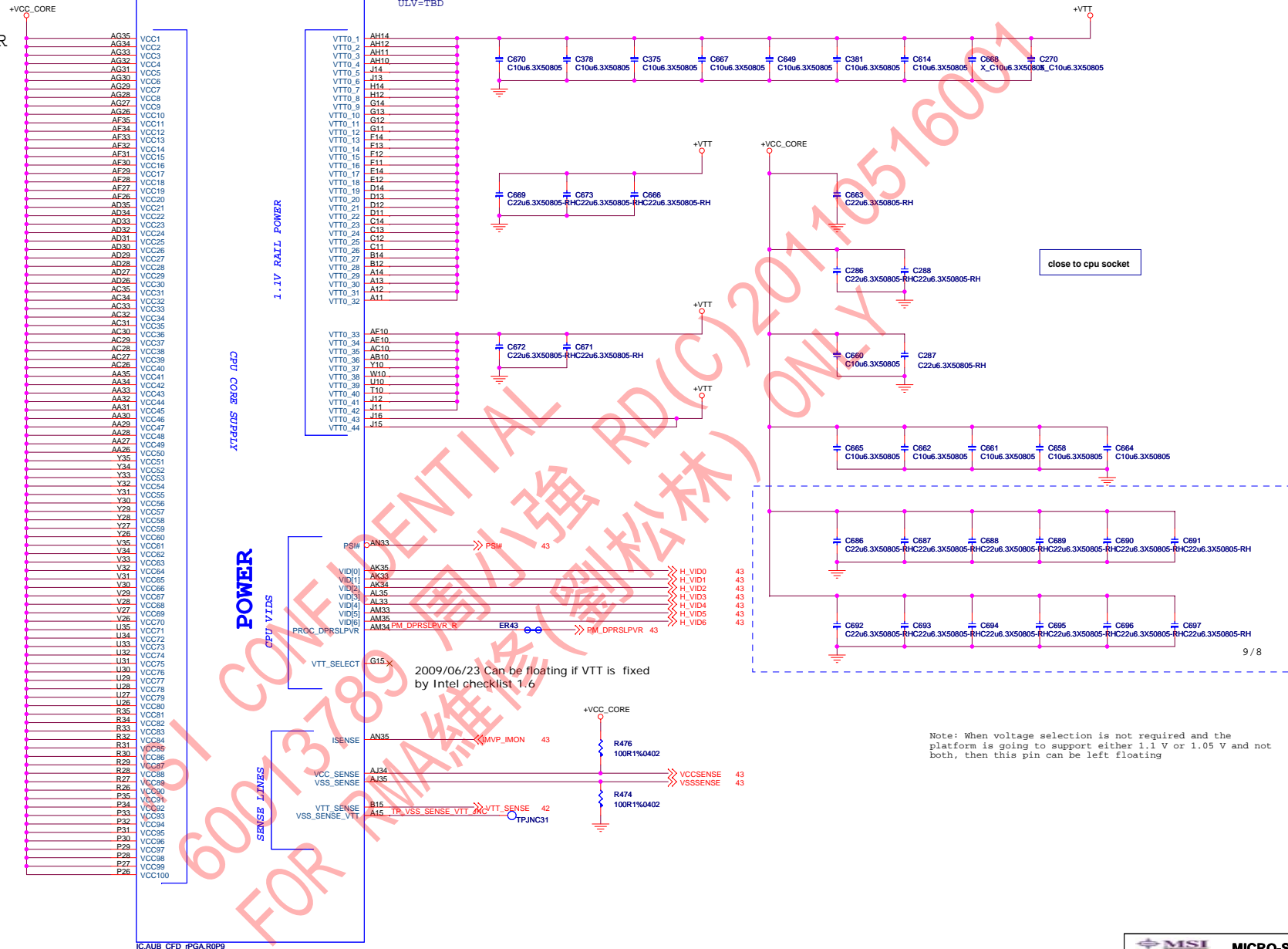
ARRANDALE:
SV=48A
LV=35A
ULV=27A

U44F

ARRANDALE:
SV=18A
LV=TBD
ULV=TBD

PROCESSOR CORE POWER

PROCESSOR CORE POWER

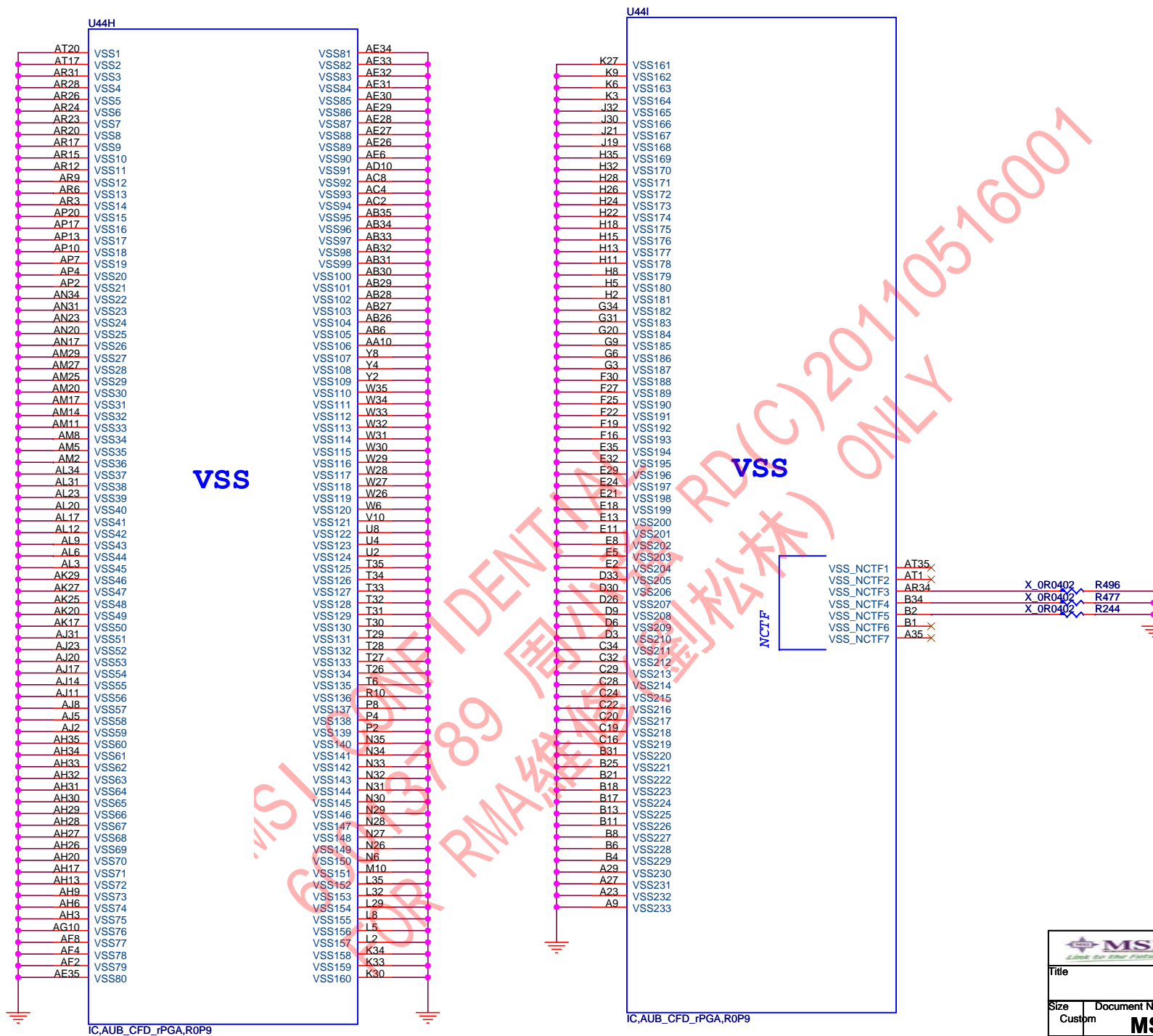


Note: When voltage selection is not required and the platform is going to support either 1.1 V or 1.05 V and not both, then this pin can be left floating

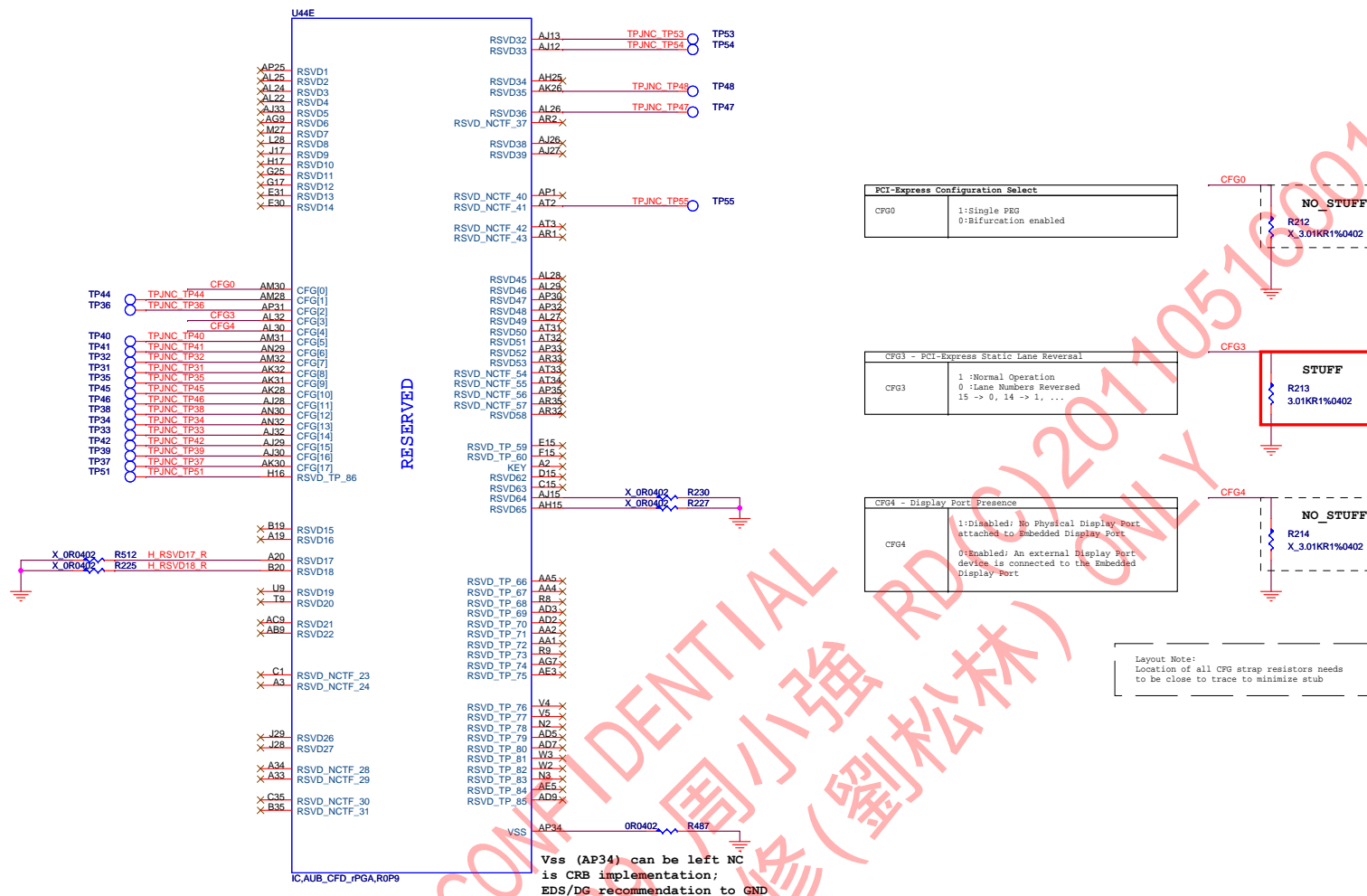
IC_AUB_CFD_TPGA_R0P9



ARRANDALE PROCESSOR (GND)



ARRANDALE PROCESSOR (RESERVED)



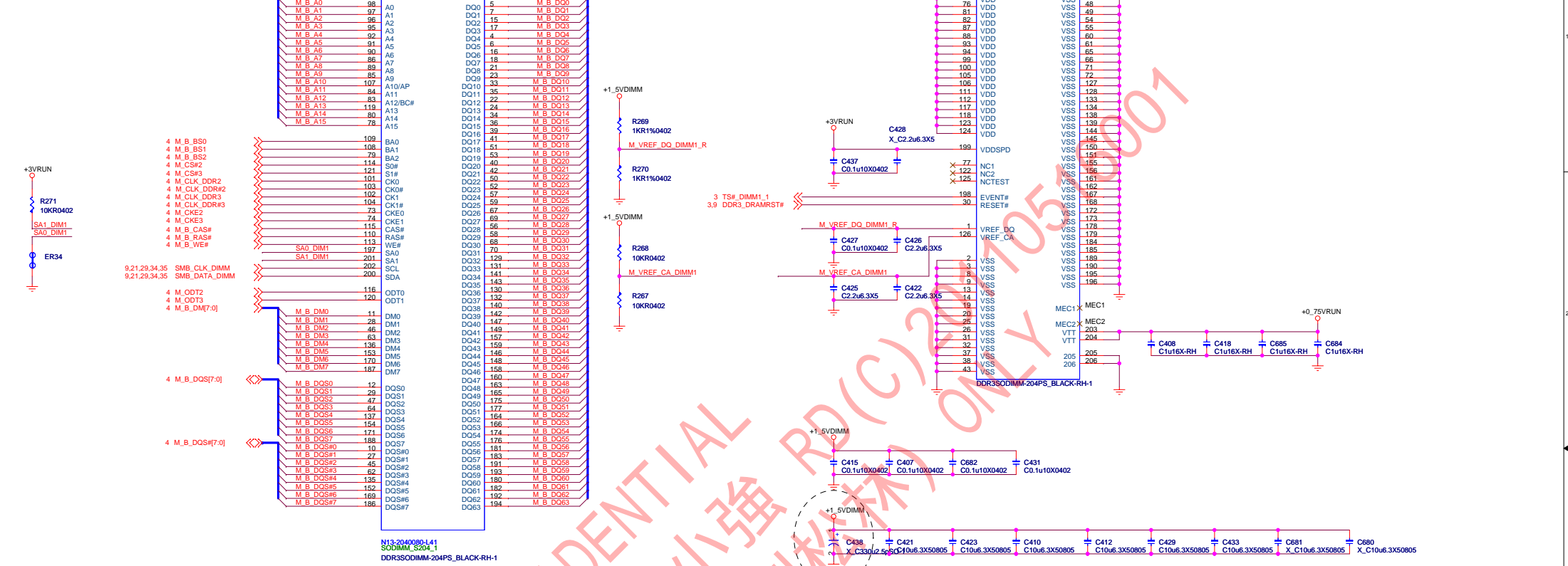
CFG[3] - PCI Express* Static Lane Numbering Reversal. Lane Reversal will be applied across all 16 Lanes.

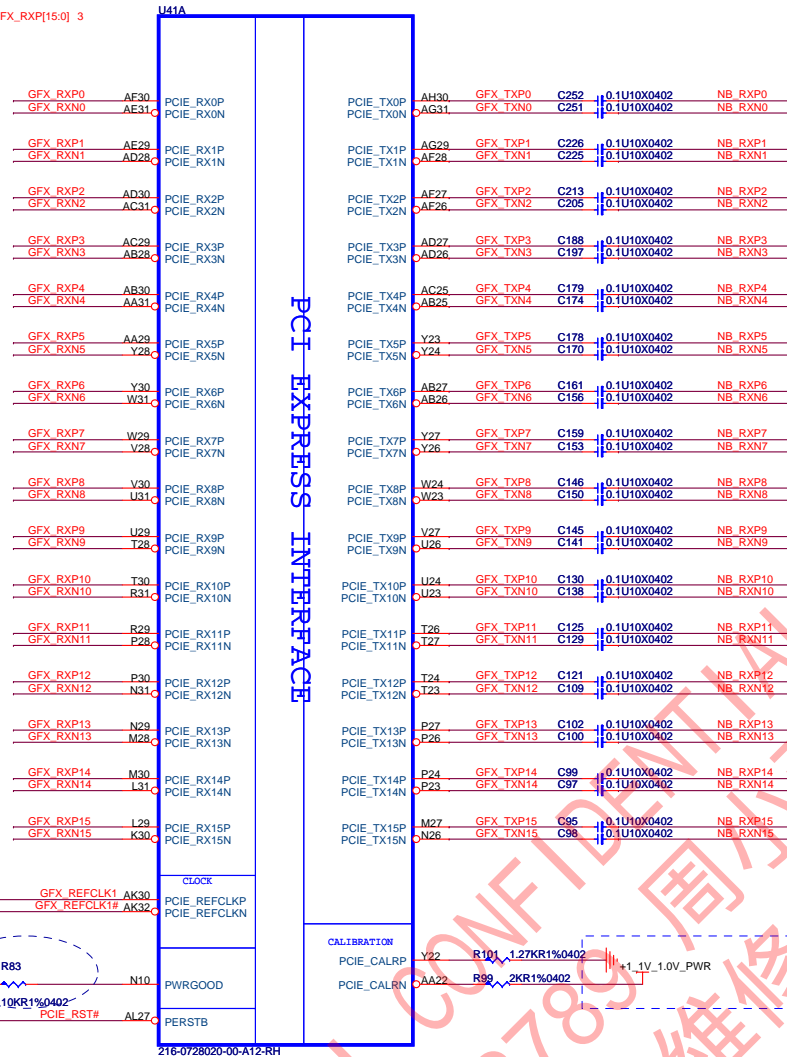
- 1: No lane reversal
- 0: Reversal

SODIMM#A

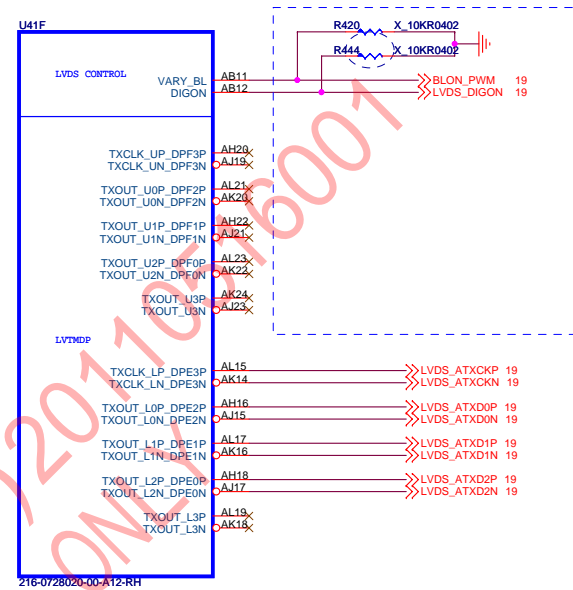


SODIMM#B

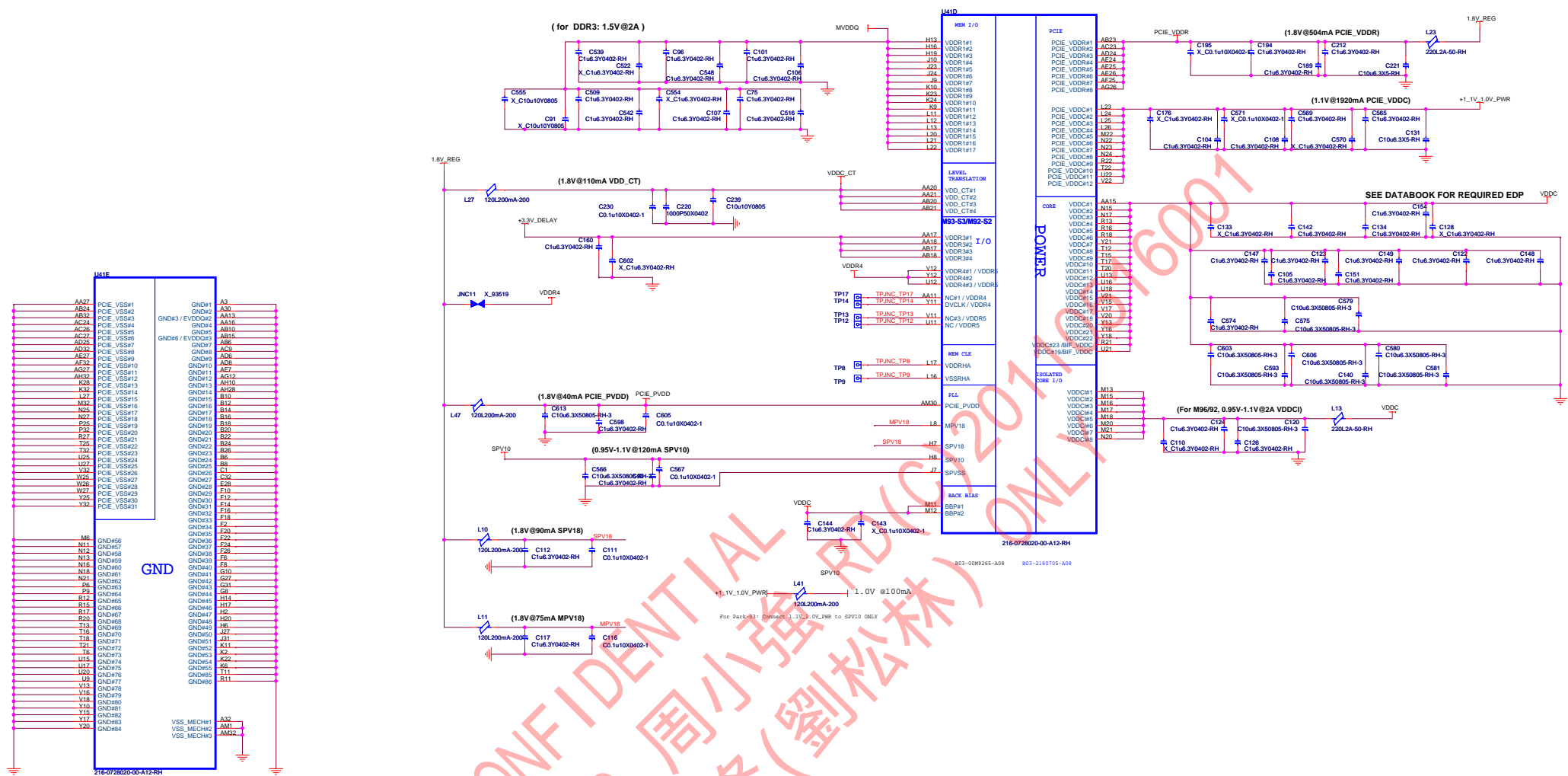




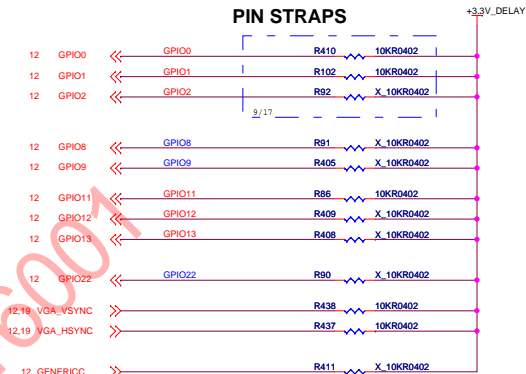
LVDS Interface



DisplayPort E Configuration



| MSI CORPORATION | | | |
|-----------------|---------------------------|-------|----------|
| File | PARK-POWER | | |
| Size | Document Number | Rev | |
| Custom | MS-1688 | 1.0 | |
| Date | Tuesday, October 06, 2009 | Sheet | 13 of 64 |



**ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED,
THEY MUST NOT CONFLICT DURING RESET**

| STRAPS | PIN | DESCRIPTION OF DEFAULT SETTINGS | |
|----------------------|----------------|--|-------|
| TX_PWRS_ENB | GPIO0 | PCIE FULL TX OUTPUT SWING | X |
| TX_DEEMPH_EN | GPIO1 | PCIE TRANSMITTER DE-EMPHASIS ENABLED | X |
| BIF_GEN2_EN_A | GPIO2 | PCIE GEN2 ENABLED | X |
| RSVD | GPIO8 | | 0 |
| BIF_VGA_DIS | GPIO9 | VGA ENABLED | 0 |
| RSVD | GPIOC1 | | 0 |
| BIOS_ROM_EN | GPIO_22_ROMCSB | ENABLE EXTERNAL BIOS ROM | X |
| ROMIDCFG(2:0) | GPIO[13:11] | SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT | X X X |
| VIP_DEVICE_STRAP_ENA | V2SYN | IGNORE VIP DEVICE STRAPS | X |
| RSVD | GENERICC | | 0 |
| AUD[1] | HSYN2 | AUD[1] AUD[0] | 0 |
| AUD[0] | VSYN | 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI | X X |

| GPIO 13, 12, 11 | |
|--------------------------------------|-------------|
| Size of the primary memory apertures | CONFIG[2:0] |
| 128 MB | 000 |
| 256 MB | 001 |
| 64 MB | 010 |
| 512 MB ^{1 GB} | 001 |

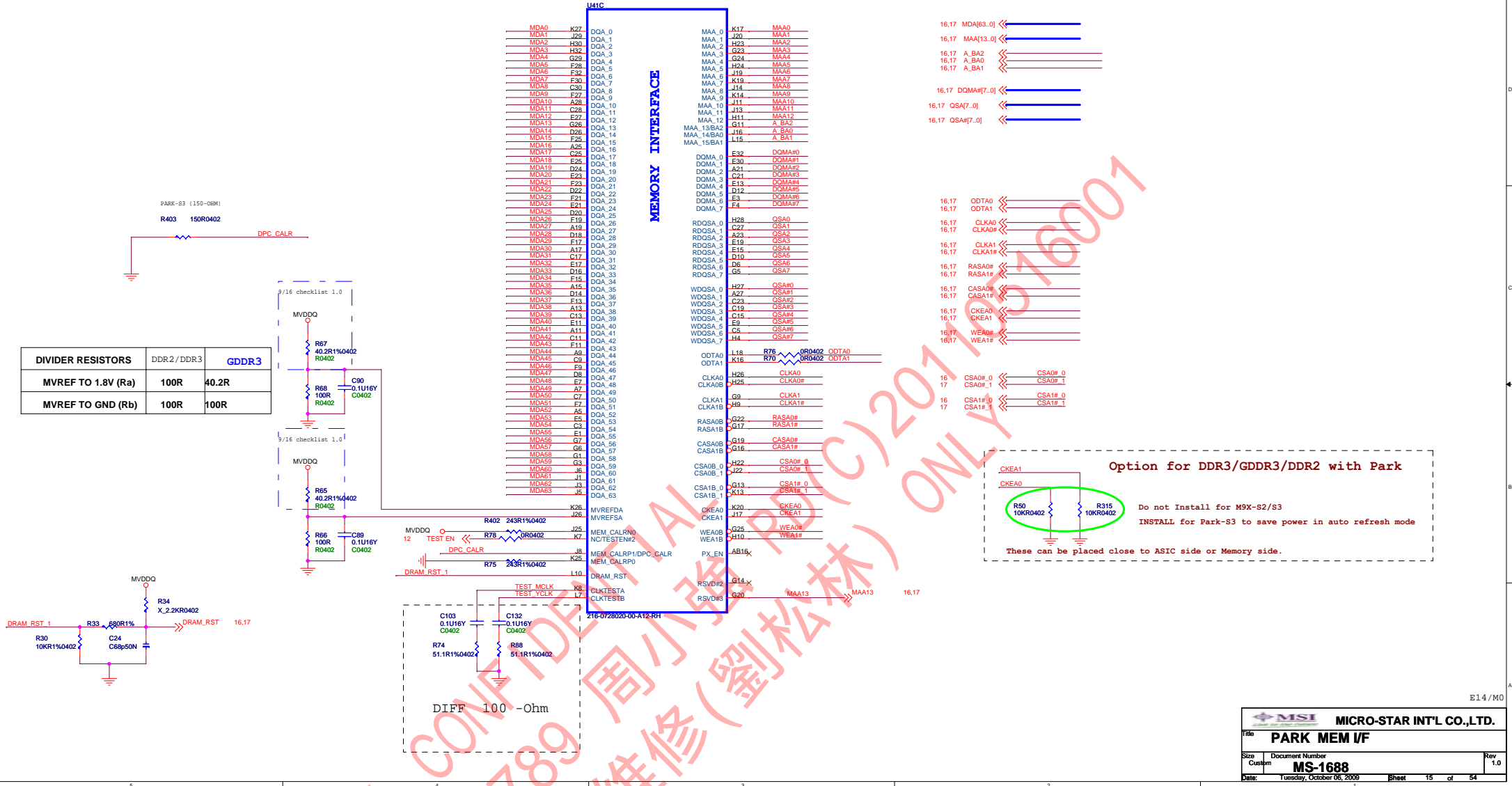
Due to memory management constraints, the aperture size should be the same size as the frame buffer for 64 MB, 128 MB and 256 MB. For frame buffers larger than 256 MB (e.g. 512 MB, 1 GB) the aperture size should be 256 MB.

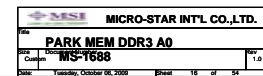
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

| | |
|--|----------|
| H2SYNC | GENERICC |
| <p>PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET</p> | |
| <p>GPI021_BB_EN</p> | |

E23/M0

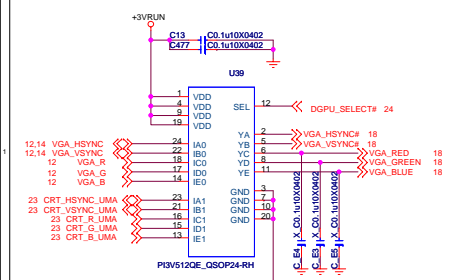
| | | | |
|--------------------------|---------------------------|-------|----------|
| Title | | | |
| PARK-power straps | | | |
| Size | Document Number | Rev | |
| Custom | MS-1688 | 1 | |
| Date: | Tuesday, October 06, 2009 | Sheet | 14 of 54 |





CRT Switch

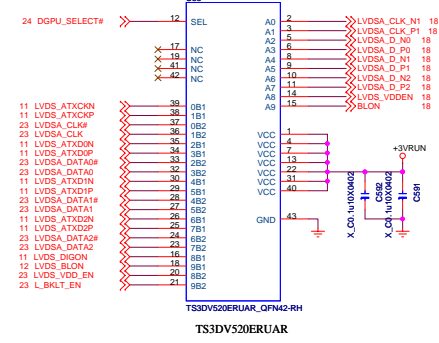
2009/07/14 Change RGB SW



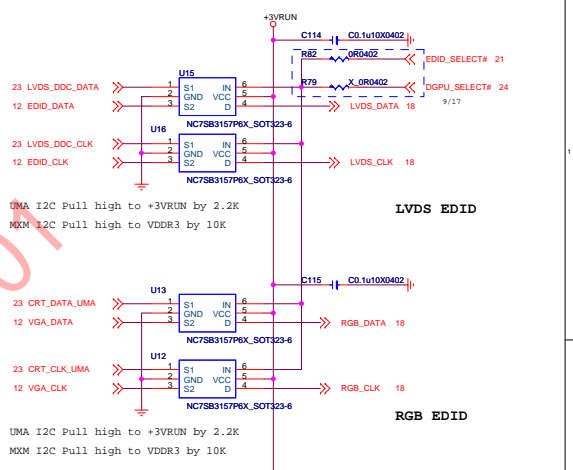
| Logic Input | Function |
|-------------|----------|
| 0 | S2 PORT |
| 1 | S1 PORT |

| BR-ADJ | |
|------------|----------------------------|
| MXM only | 1. MXM 2. EC |
| Switchable | 1. MXM 2. iGPU 3. EC |

LVDS Switch



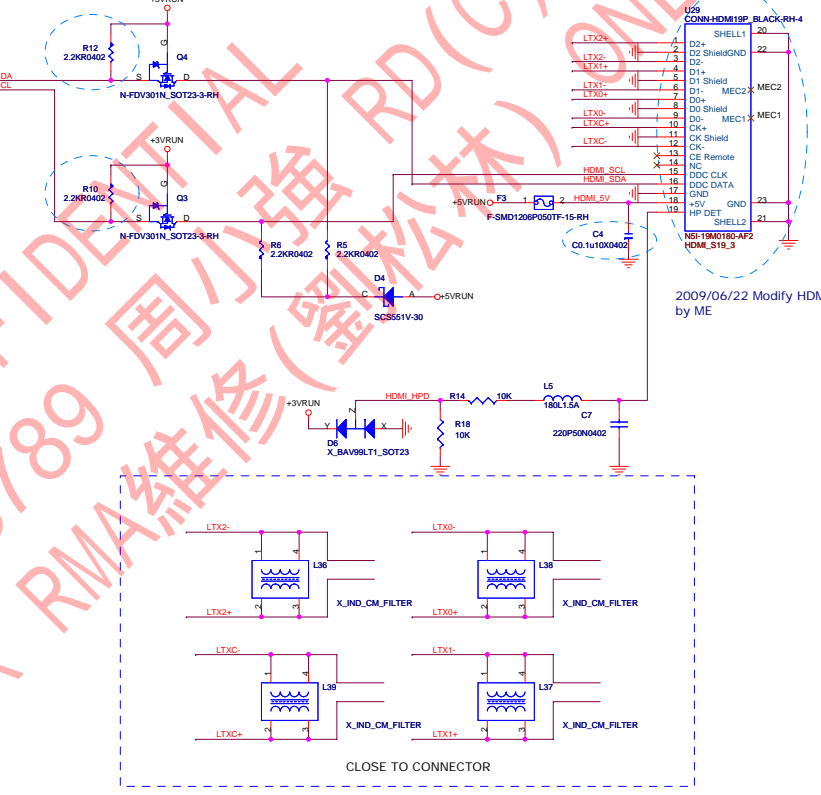
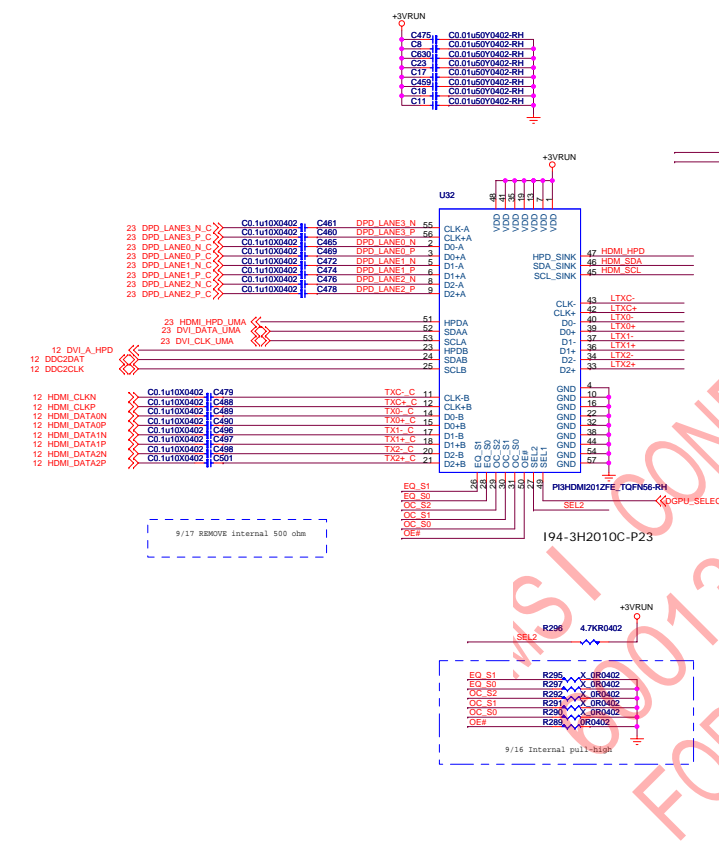
EDID Switch (CRT, LVDS)



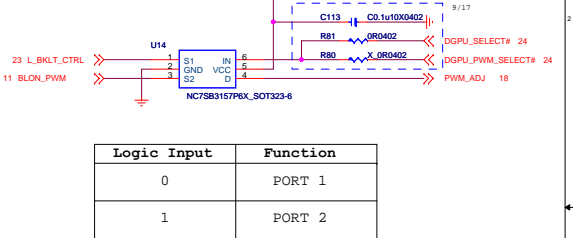
HDMI Switch

2009/07/14 Change HDMI SW

| Logic Input | Function |
|-------------|----------|
| 0 | B PORT |
| 1 | A PORT |

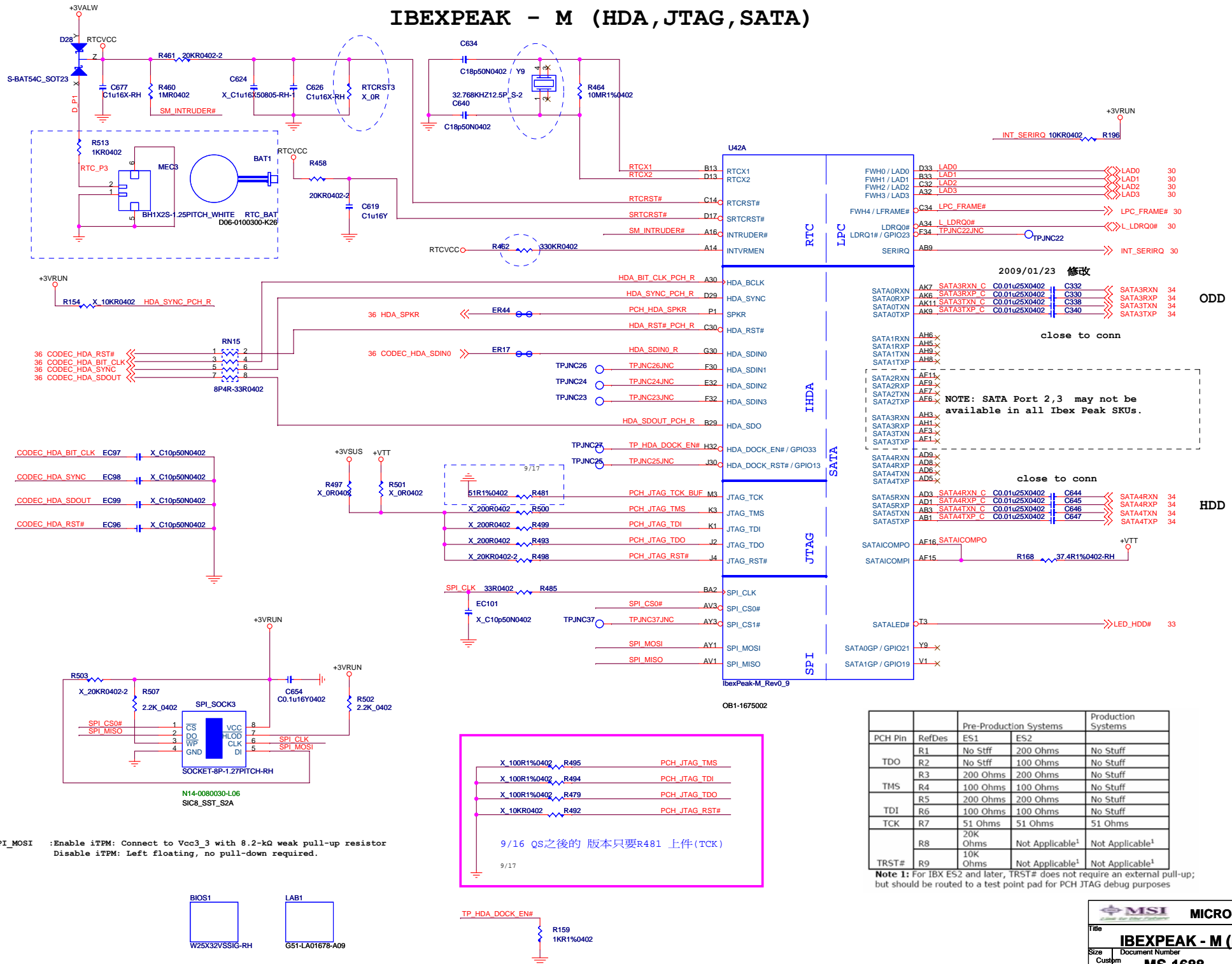


2009/07/14 DEL HDMI I2C SW (U26, U27)



| Logic Input | Function |
|-------------|----------|
| 0 | PORT 1 |
| 1 | PORT 2 |

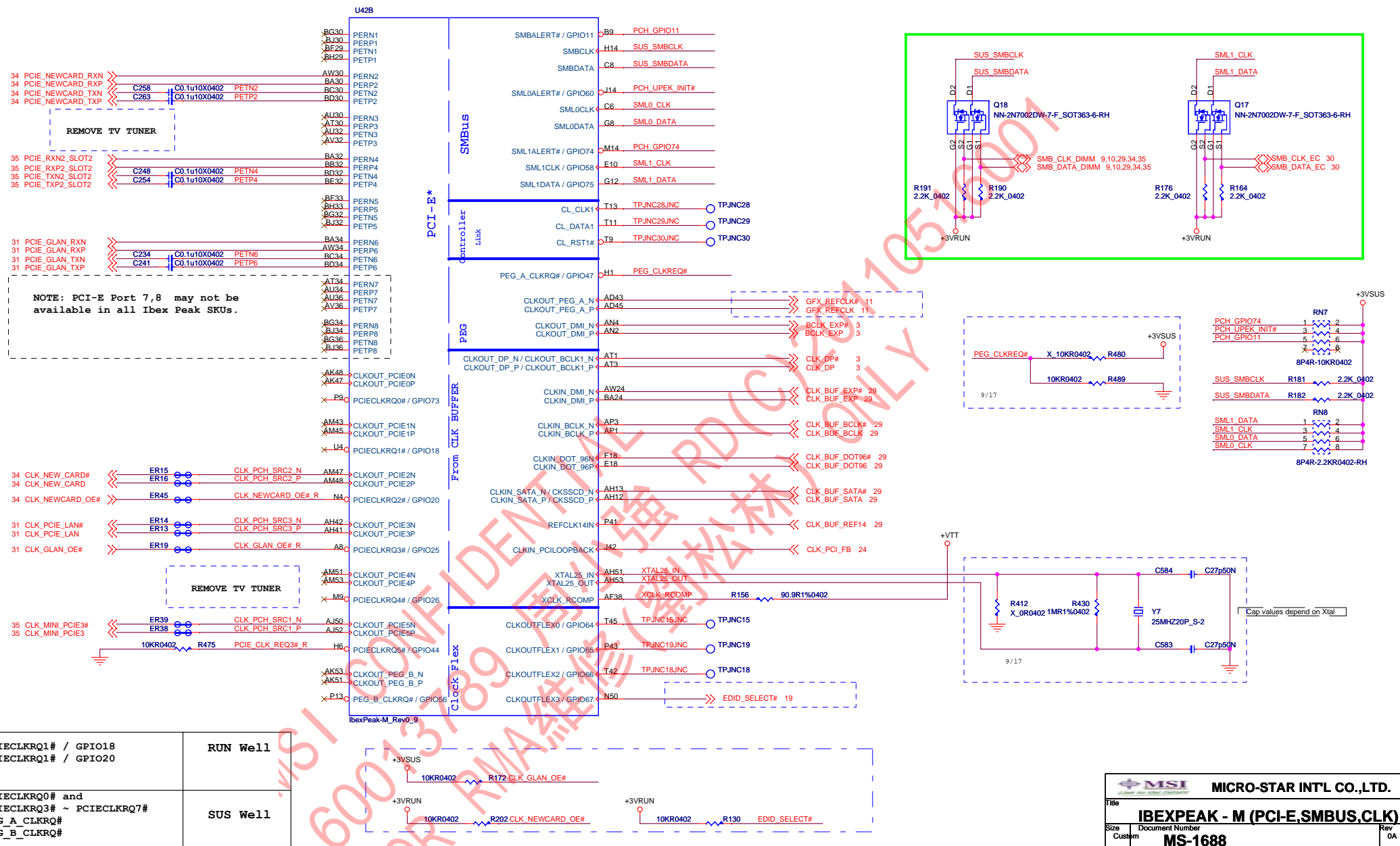
IBEXPEAK - M (HDA, JTAG, SATA)



| | | Pre-Production Systems | | Production Systems |
|---------|--------|------------------------|-----------------------------|-----------------------------|
| PCH Pin | RefDes | ES1 | ES2 | |
| TDO | R1 | No Stff | 200 Ohms | No Stuff |
| | R2 | No Stff | 100 Ohms | No Stuff |
| | R3 | 200 Ohms | 200 Ohms | No Stuff |
| TMS | R4 | 100 Ohms | 100 Ohms | No Stuff |
| | R5 | 200 Ohms | 200 Ohms | No Stuff |
| TDI | R6 | 100 Ohms | 100 Ohms | No Stuff |
| TCK | R7 | 51 Ohms | 51 Ohms | 51 Ohms |
| TRST# | R8 | 20K Ohms | Not Applicable ¹ | Not Applicable ¹ |
| | R9 | 10K Ohms | Not Applicable ¹ | Not Applicable ¹ |

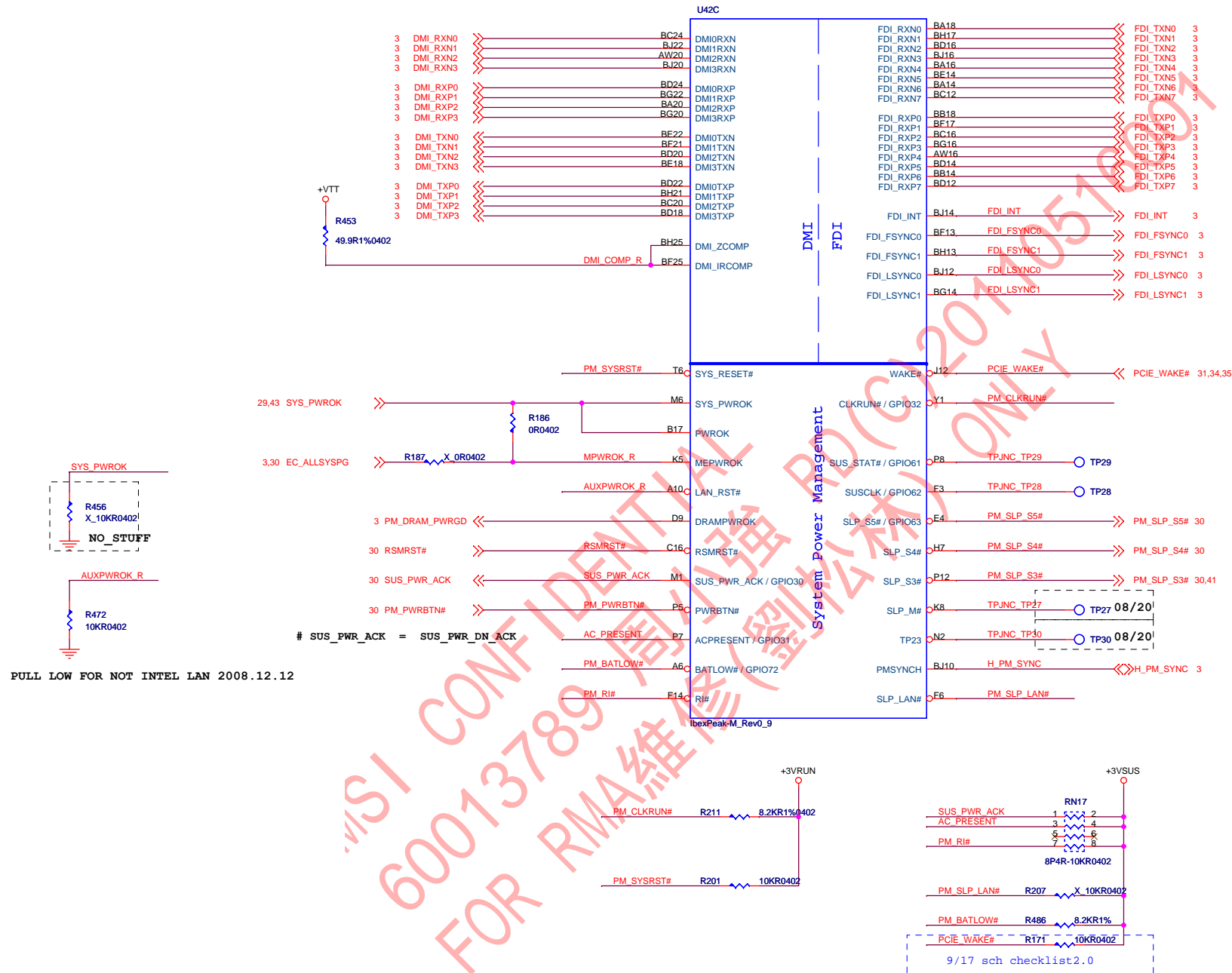
Note 1: For IBX ES2 and later, TRST# does not require an external pull-up; but should be routed to a test point pad for PCH JTAG debug purposes

IBEXPEAK - M (PCI-E, SMBUS, CLK)

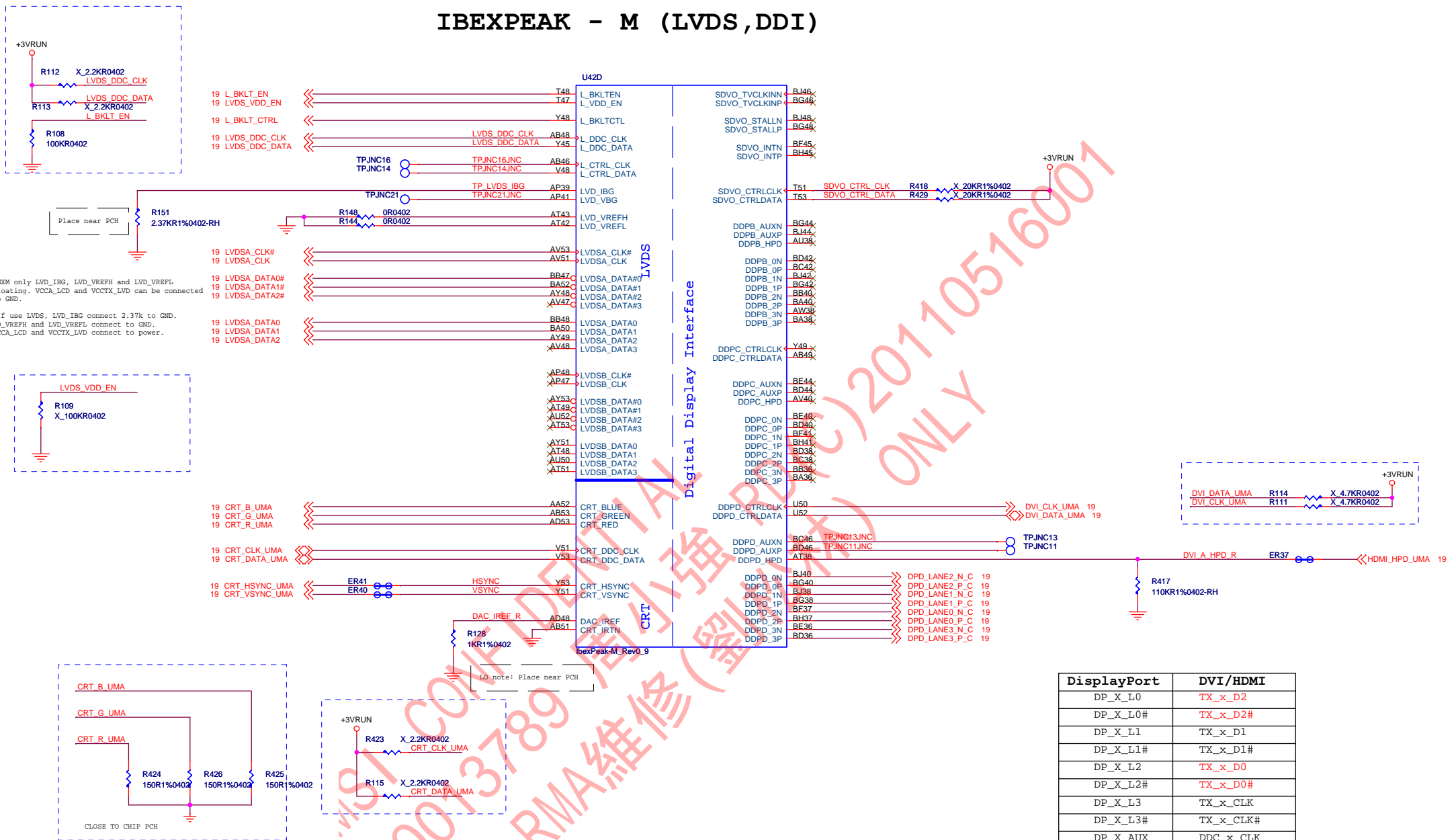


| | |
|--|----------|
| PCIECLKRQ1# / GPIO18 PCIECLKRQ1# / GPIO20 | RUN Well |
| PCIECLKRQ0# and PCIECLKRQ3# ~ PCIECLKRQ7# PEG_A_CLKRQ# PEG_B_CLKRQ# | SUS Well |

IBEXPEAK - M (DMI, FDI, GPIO)



IBEXPEAK - M (LVDS,DDI)

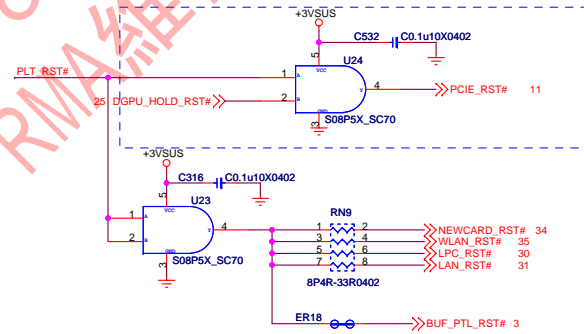
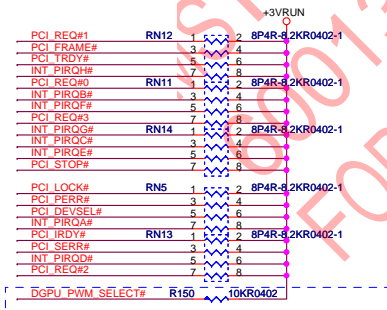
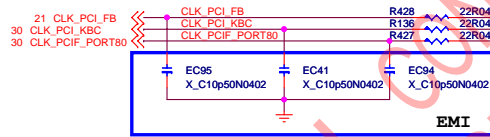
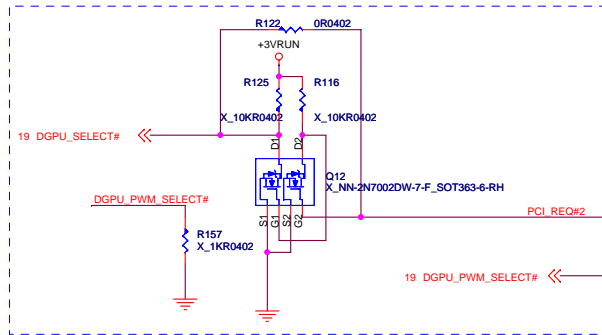
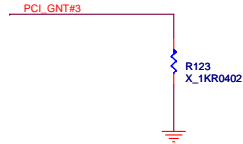
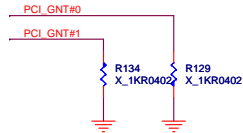


| DisplayPort | DVI/HDMI |
|-------------|------------|
| DP_X_L0 | TX_x_D2 |
| DP_X_L0# | TX_x_D2# |
| DP_X_L1 | TX_x_D1 |
| DP_X_L1# | TX_x_D1# |
| DP_X_L2 | TX_x_D0 |
| DP_X_L2# | TX_x_D0# |
| DP_X_L3 | TX_x_CLK |
| DP_X_L3# | TX_x_CLK# |
| DP_X_AUX | DDC_x_CLK |
| DP_X_AUX# | DDC_x_DATA |

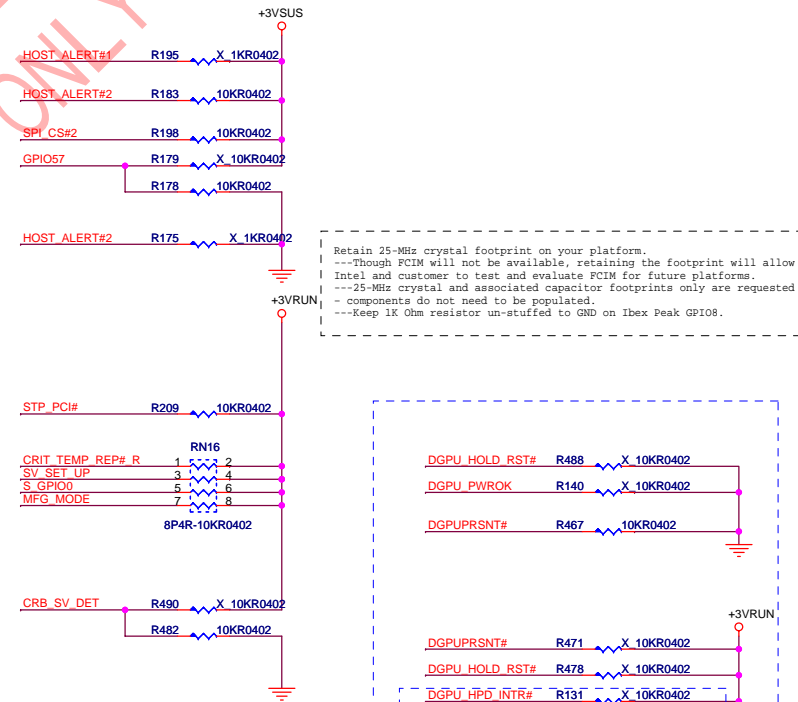
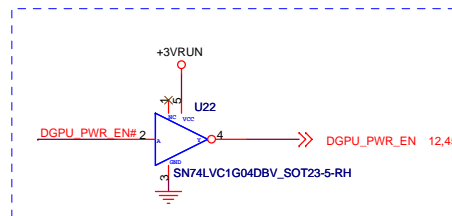
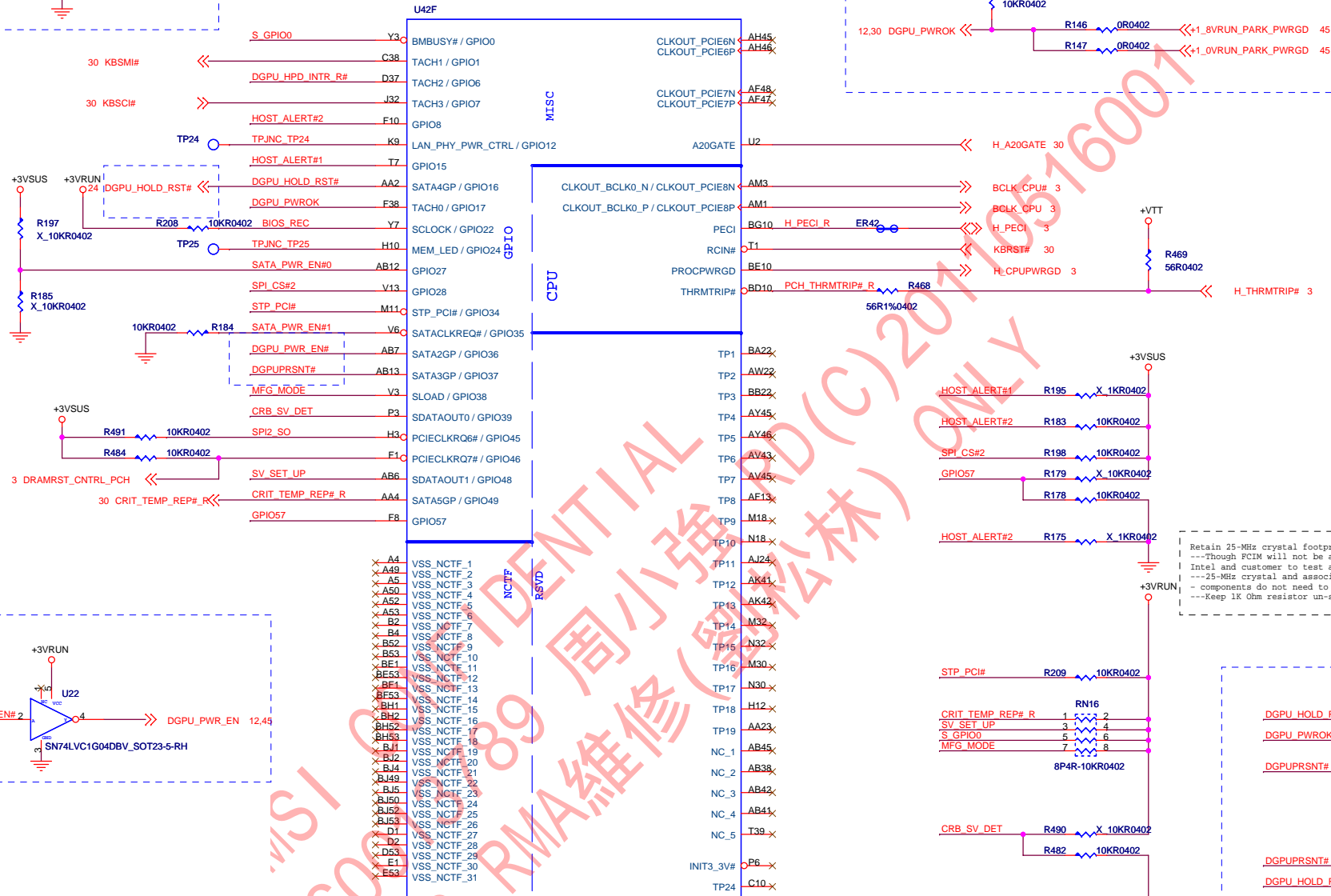
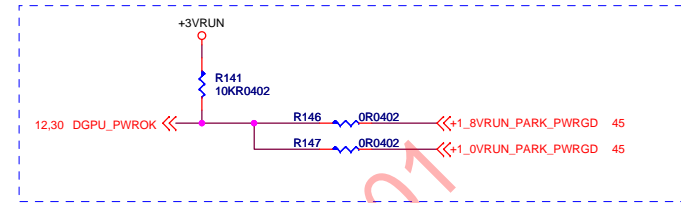
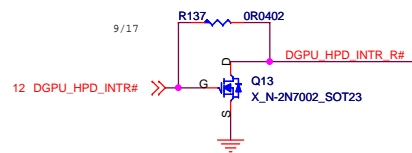
IBEXPEAK - M (PCI,USB,NVRAM)

| Boot BIOS Strap | | |
|-----------------|-----------|--------------------|
| PCI_GNT#0 | PCI_GNT#1 | Boot BIOS Location |
| 0 | 0 | LPC |
| 0 | 1 | Reserved |
| 1 | 0 | PCI |
| 1 | 1 | SPI |

| | |
|---|---|
| A16 swap override Strap/Top-Block Swap Override jumper | |
| PCI_GNT#3 | Low = A16 swap override/Top-Block Swap Override enabled High = Default |



IBEXPEAK - M (GPIO,VSS_NCTF,RSVD)

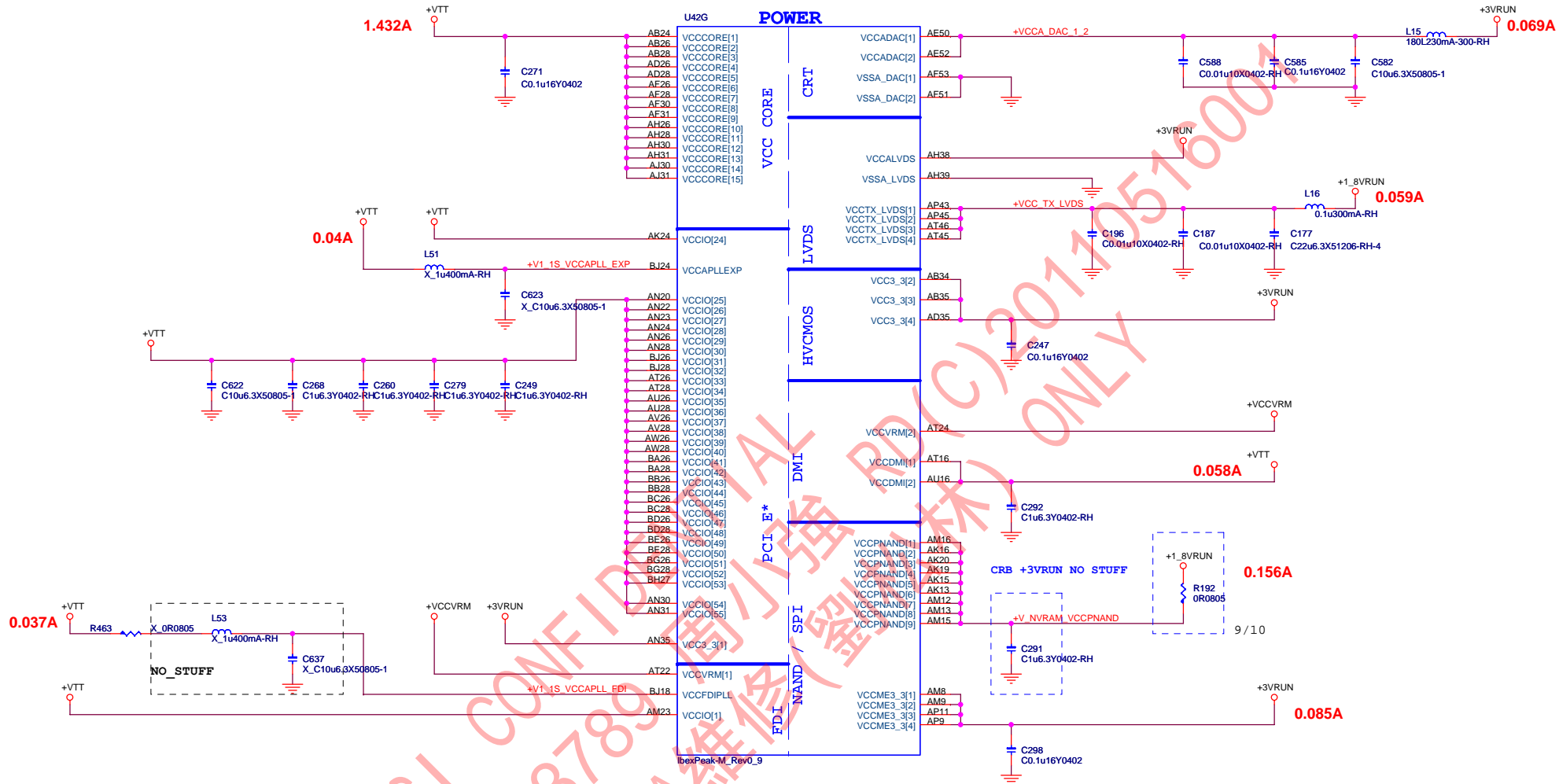


```

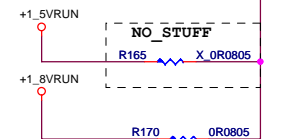
| Retain 25-MHz crystal footprint on your platform.
| ---Though FCIM will not be available, retaining the footprint will allow
| Intel and customer to test and evaluate FCIM for future platforms.
| ---25-MHz crystal and associated capacitor footprints only are requested
N| - components do not need to be populated.
| ---Keep 1K Ohm resistor un-stuffed to GND on Ibox Peak GPIO8.

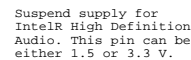
```

IBEXPEAK - M (POWER)

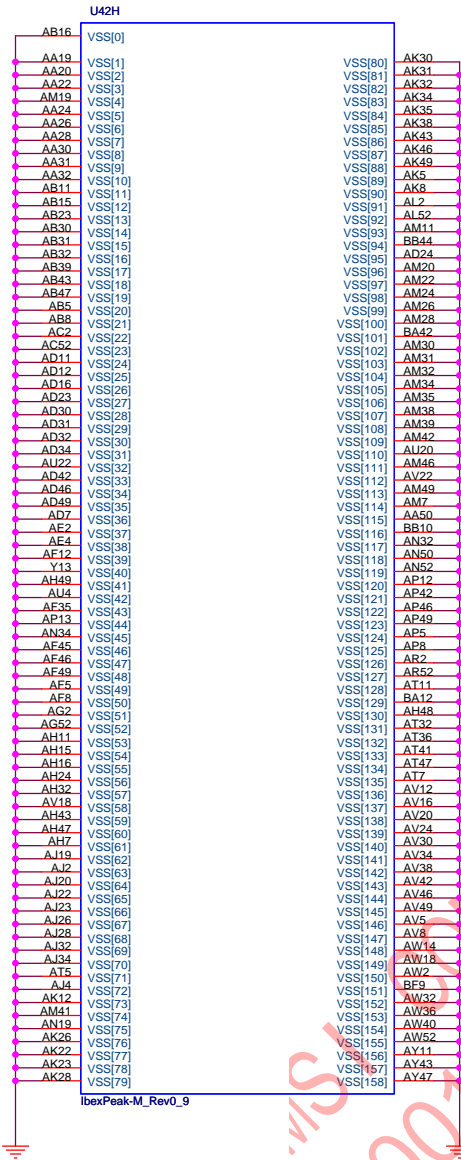


The VCCVCRM rail (1.8 V/1.5 V) powers an internal voltage regulator module (VRM) that regulates clean 1.05-V voltage supply for analog rails (VCCAClk, VccapllEXP, VCCFDIPLL, and VCCSATAPLL). This solution will allow us to remove the LC filter requirements for those rails, thereby reducing platform BOM cost. VCCVCRM is enabled by default via internal pull up to GPIO27, therefore GPIO27 should be left as No Connect. The following diagram shows implementation details on how to enable and disable VccVRM.

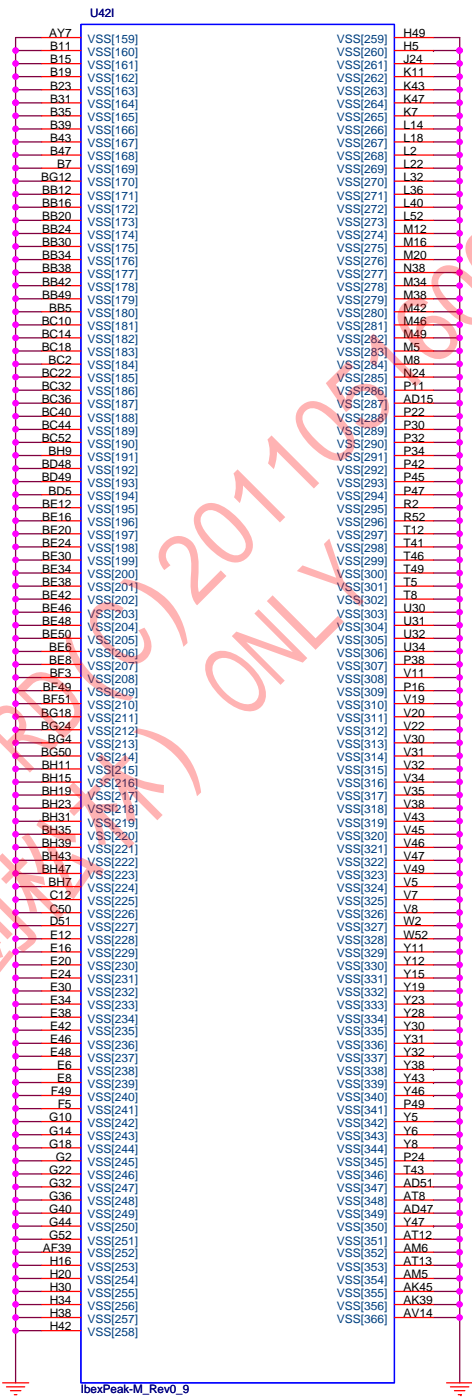


IBEXPEAK - M (POWER)

IBEXPEAK - M (GND)



IbexPeak-M_Rev0_9



IbexPeak-M_Rev0_9

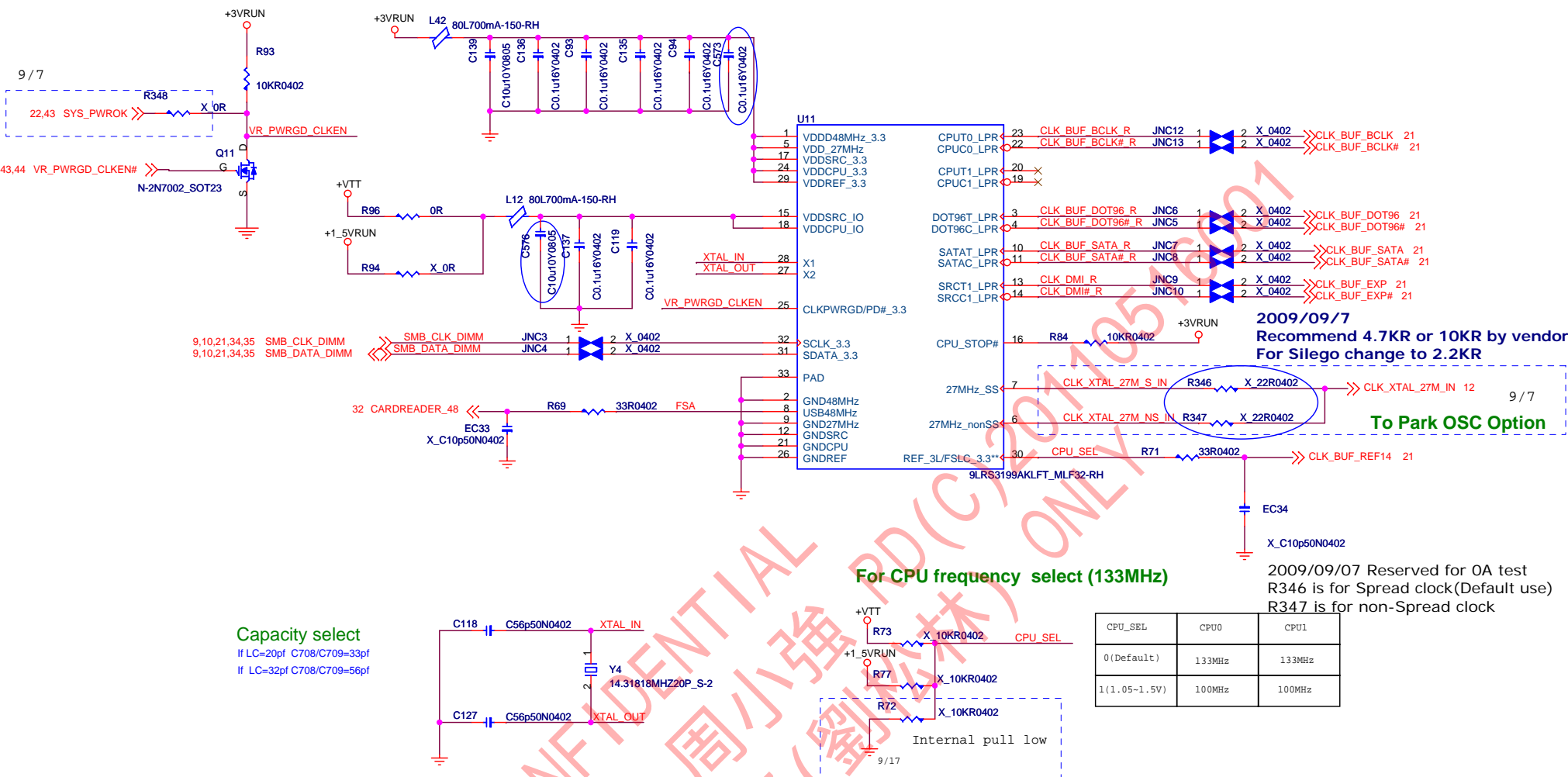
MSI
MICRO-STAR INT'L CO.,LTD.

Title
IBEXPEAK - M (GND)

Size Custom Document Number
MS-1688

Date: Tuesday, October 06, 2009 Sheet 28 of 52

Rev 0A



Capacity select
If LC=20pf C708/C709=33pf
If LC=32pf C708/C709=56pf

For CPU frequency select (133MHz)

Co-Lay Note:

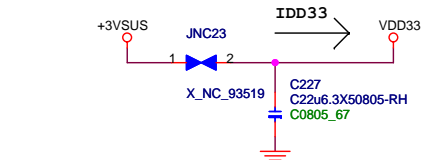
For IDT IC91RS3199
R84,R73,R71=10Kohm

For Silago SLG8SP587
R84,R73,R600=4.7Kohm

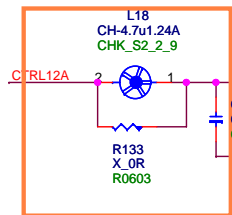
2009/09/7
Recommend 4.7KR or 10KR by vendor
For Silago change to 2.2KR

To Park OSC Option

| CPU_SEL | CPU0 | CPU1 |
|--------------|--------|--------|
| 0(Default) | 133MHz | 133MHz |
| 1(1.05~1.5V) | 100MHz | 100MHz |

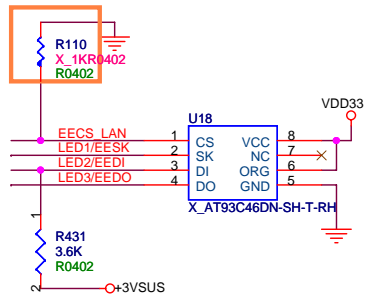


$$\begin{aligned} \text{IDD33} &= \text{Icc33} + \text{ICCL2} \\ &= 58\text{mA} + 289\text{mA} \\ &= 347\text{mA} \end{aligned}$$

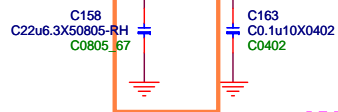


Note 1: The Trace length between L1 and 8111DL's Pin 1 must be within 0.5 cm. C171 and C181 to L18 must be within 0.5cm. Refer to Layout guide for more detail.

R110 is only required by RTL8102EL



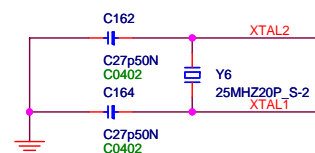
C158 is only RTL8111DL



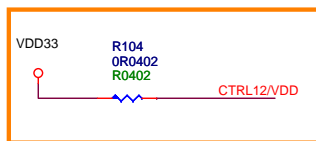
Close to LAN

pin46:2.49k close to 5 mil use ground shielding around

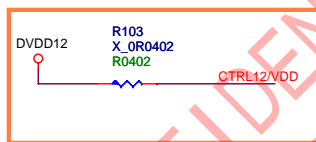
R106 is only RTL8111DL



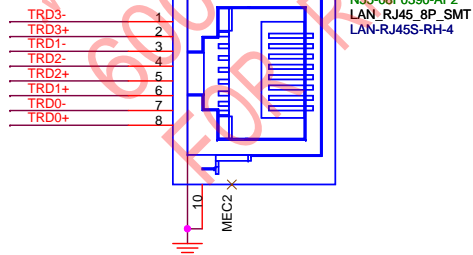
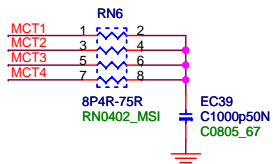
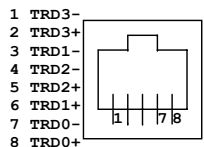
For RTL8111DL, use this block



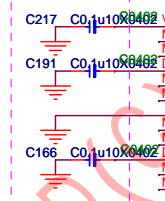
For RTL8102EL/8103EL, use this block



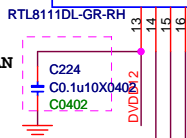
RJ45 Pin define



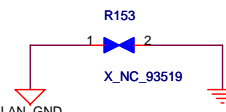
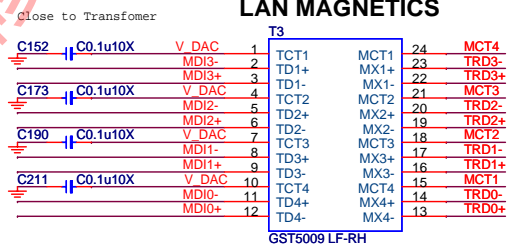
Close to LAN

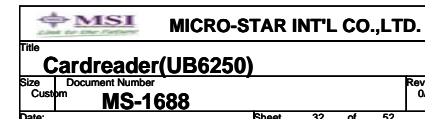


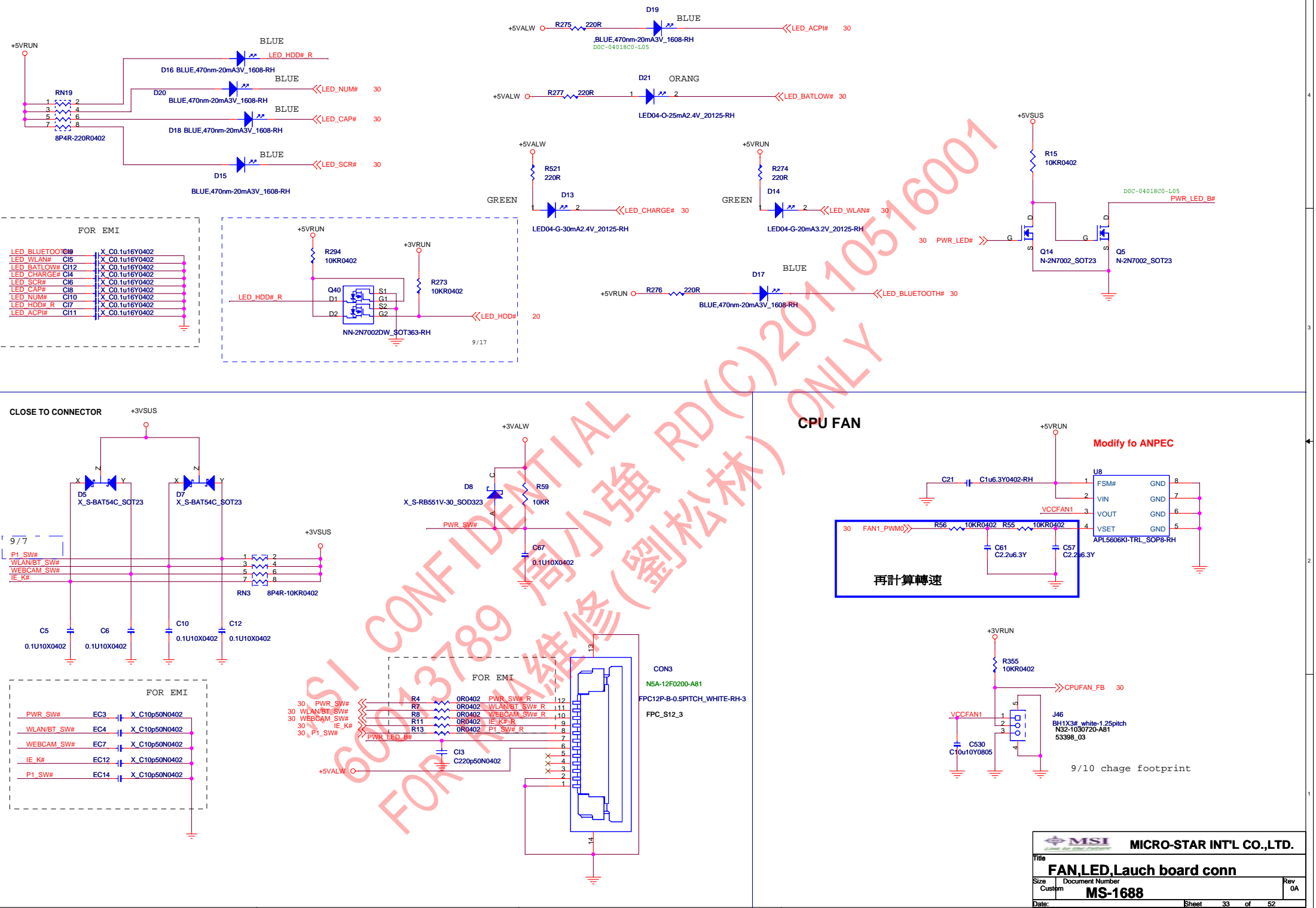
Close to LAN



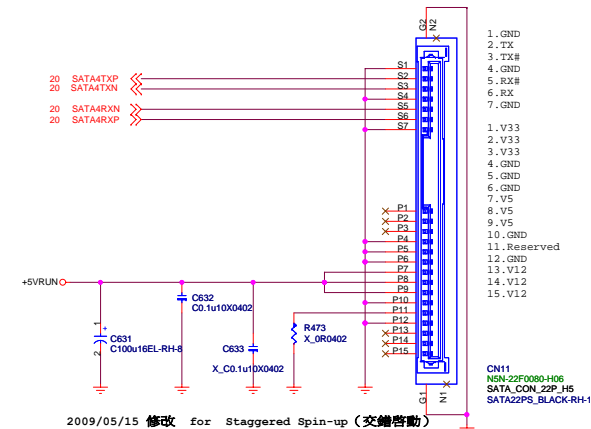
LAN MAGNETICS



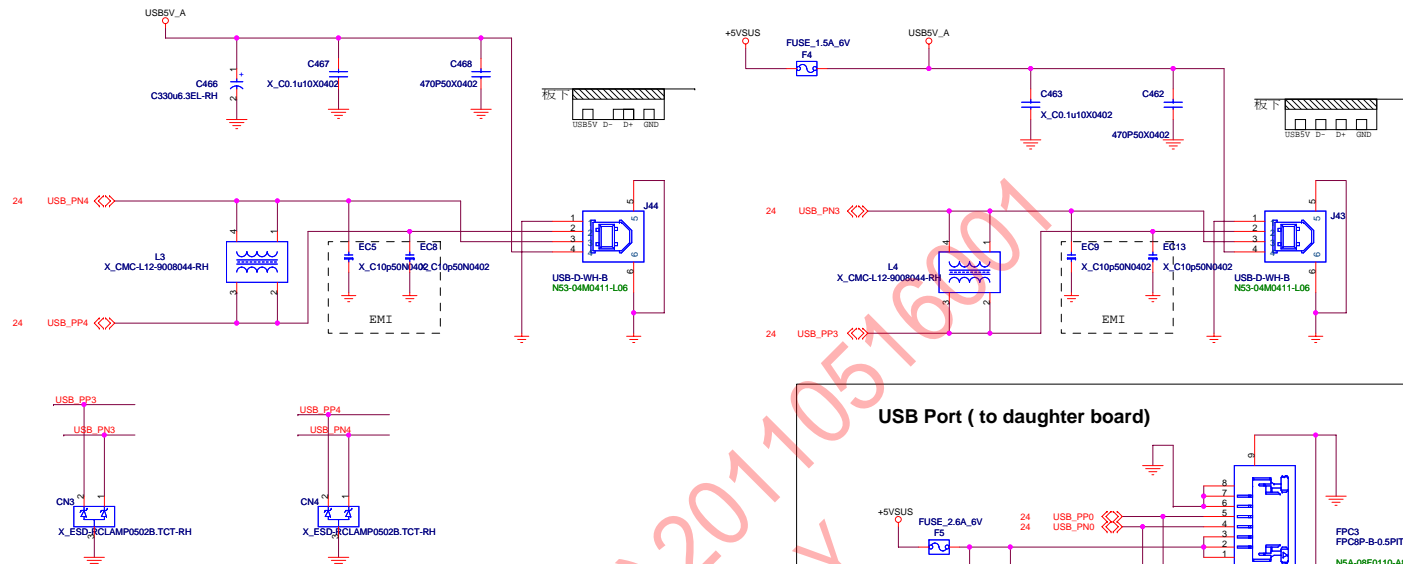




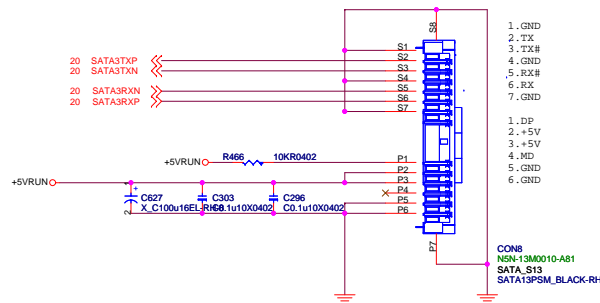
SATA HDD



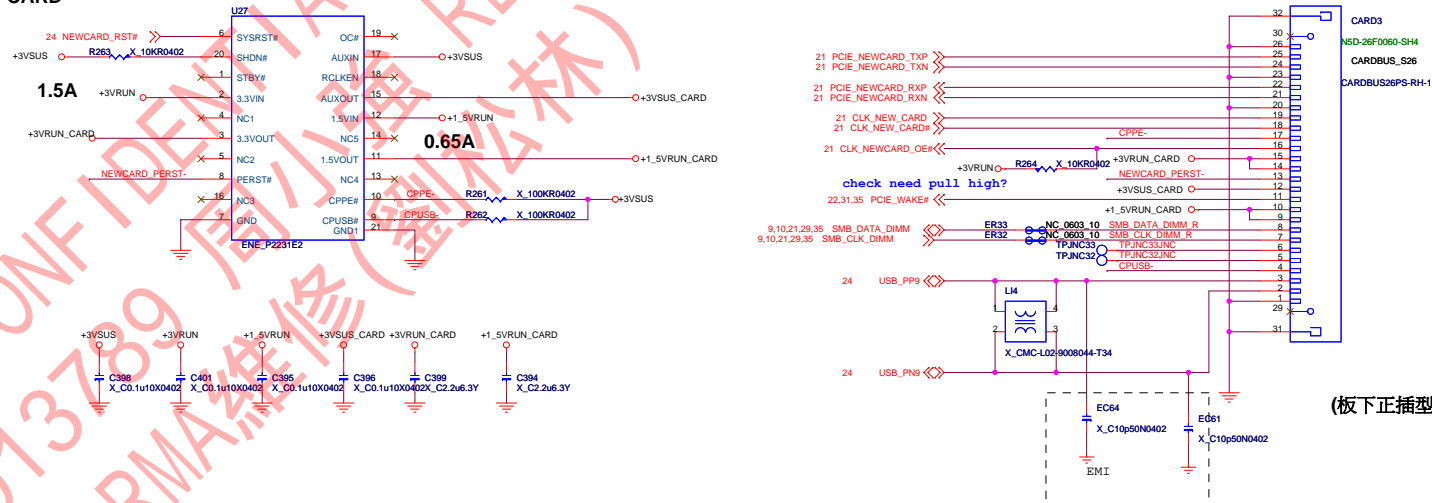
USB Port



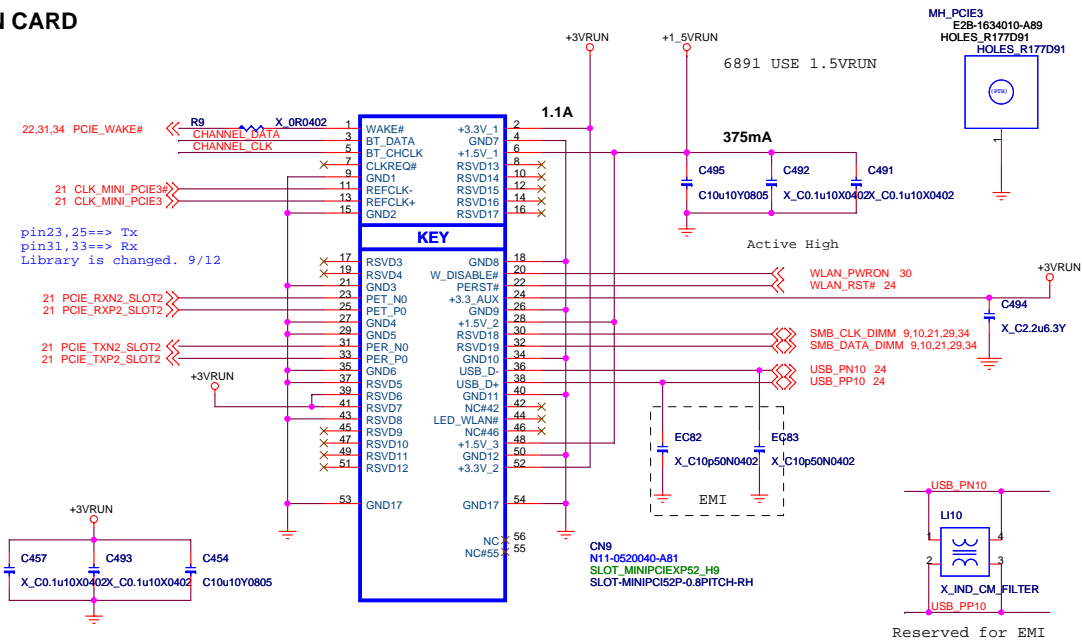
SATA ODD



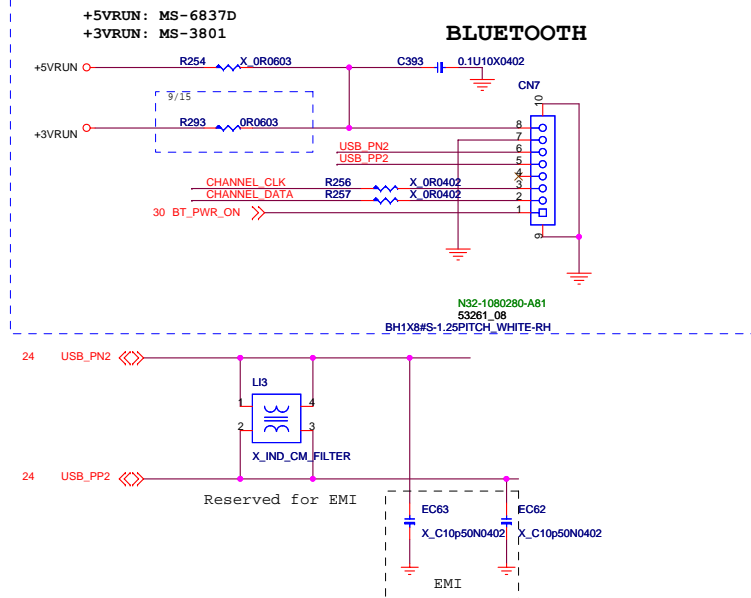
NEW CARD



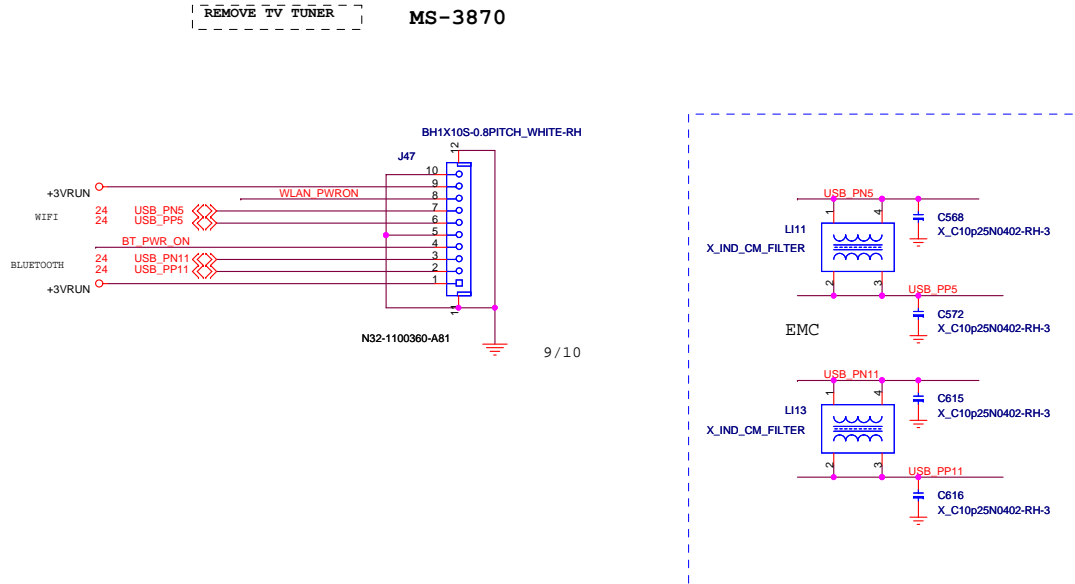
WLAN CARD



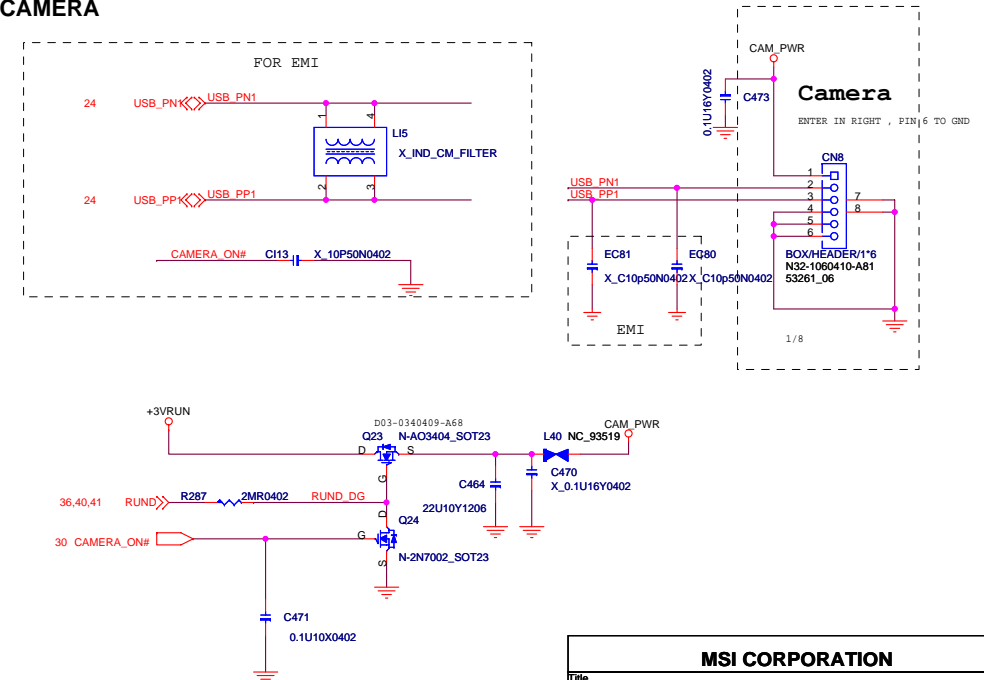
BLUETOOTH

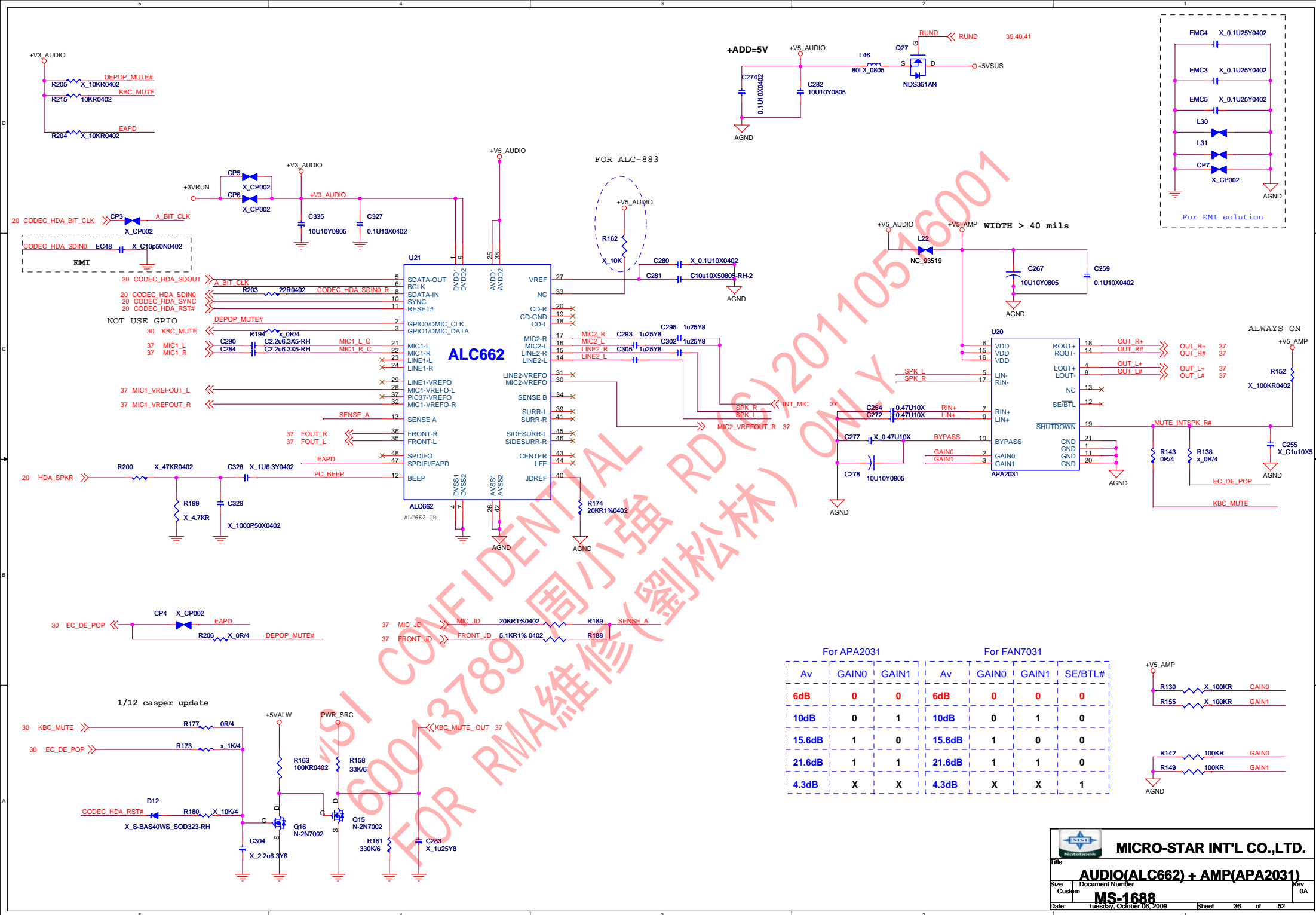


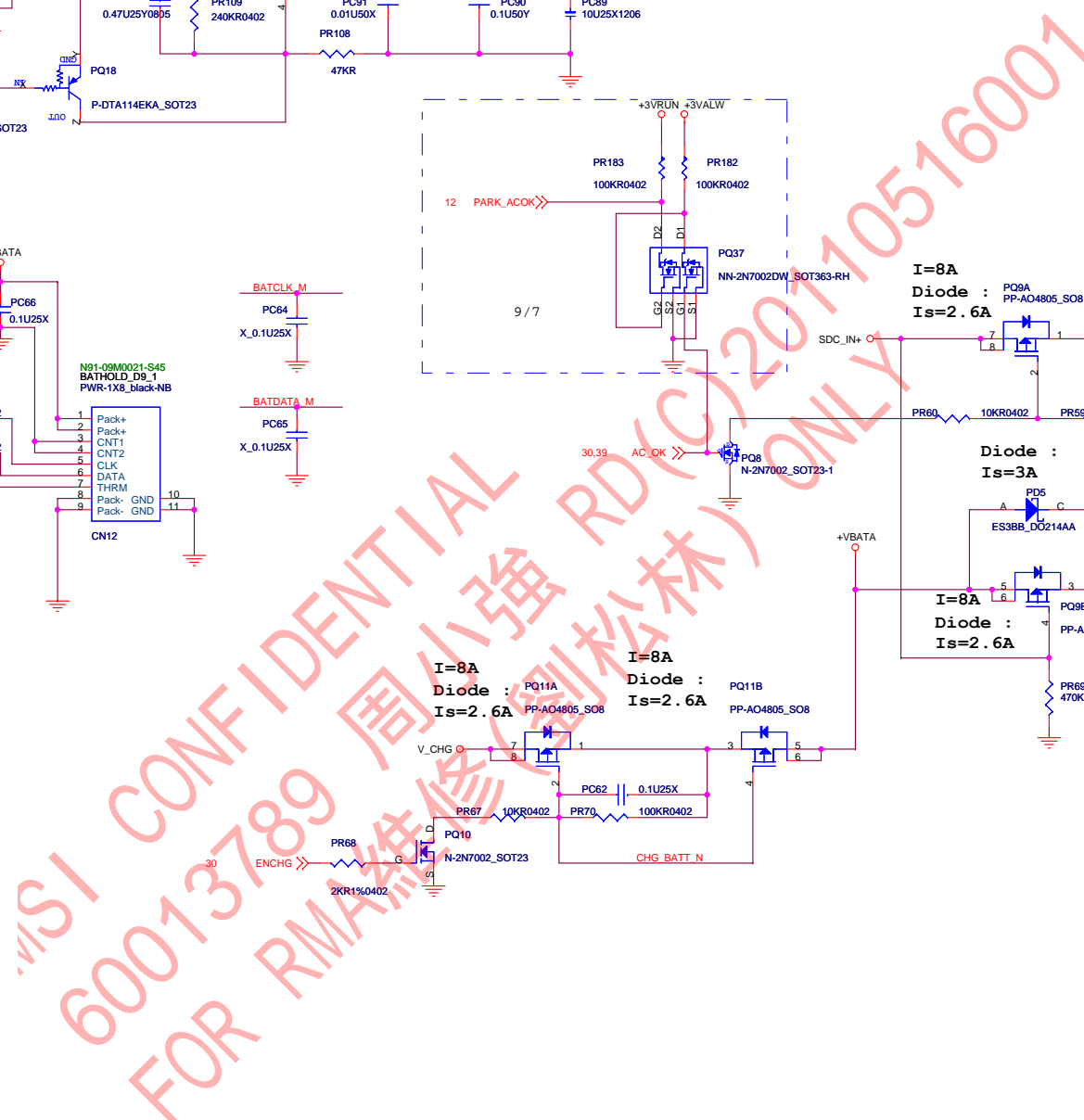
MS-3870



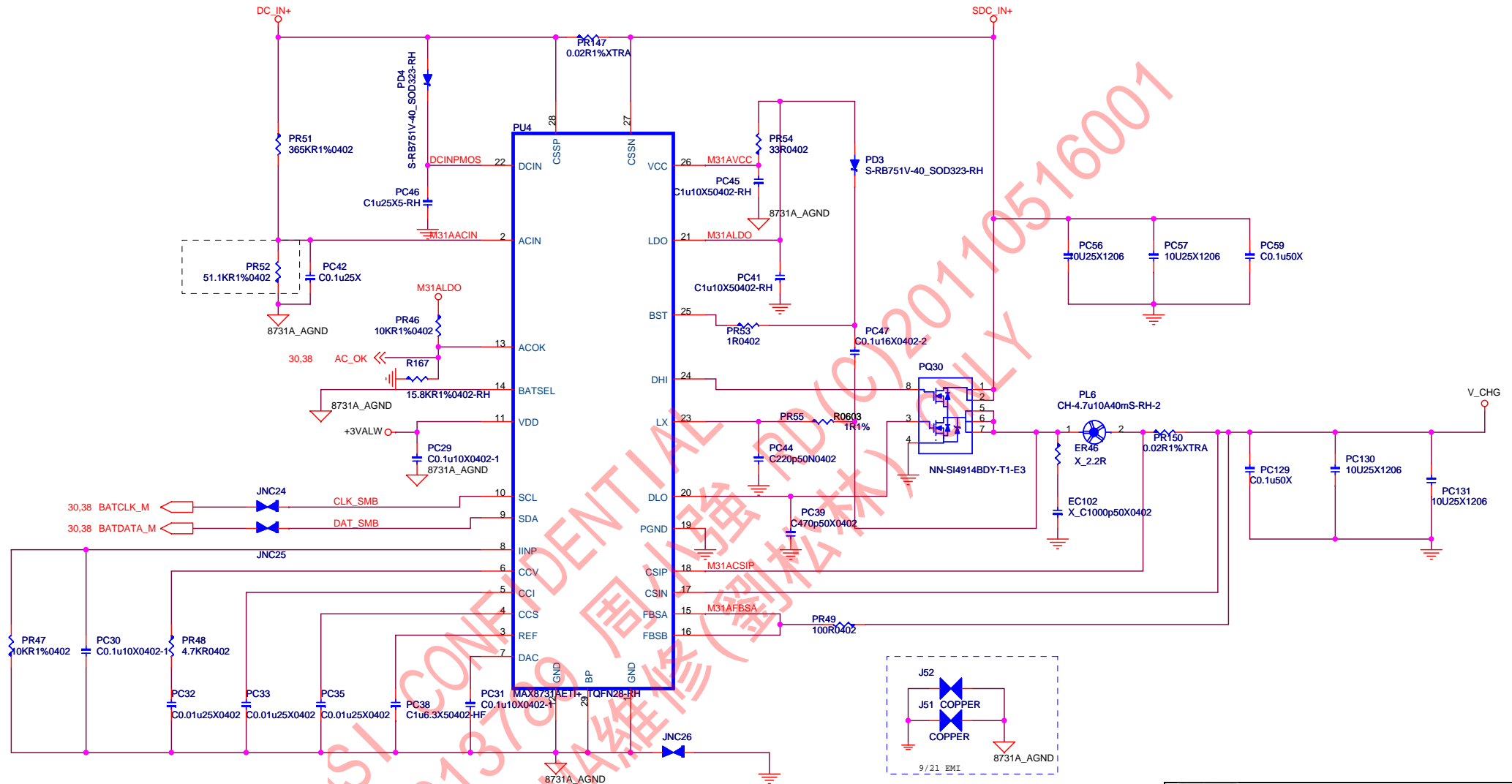
CAMERA








Adapter input voltage set 19 Voltage



IINP :

1. The transconductance from (CSSP - CSSN) to IINP is 3mA/V.
2. $V_{IINP} = IINP_{UT} \times RS1 \times 3mA/V \times PR25$

| | |
|--|--|
|  MICRO-STAR INT'L CO.,LTD. | |
| Title Battery Charger | |
| Size B Document Number Rev. 1.0 | |
| MS-1688 | |
| Date: Tuesday, October 06, 2009 Sheet 39 of 54 | |

$$ILIM = (R_{imax} \times 20\mu A / R_{dson}) + 1.82A$$

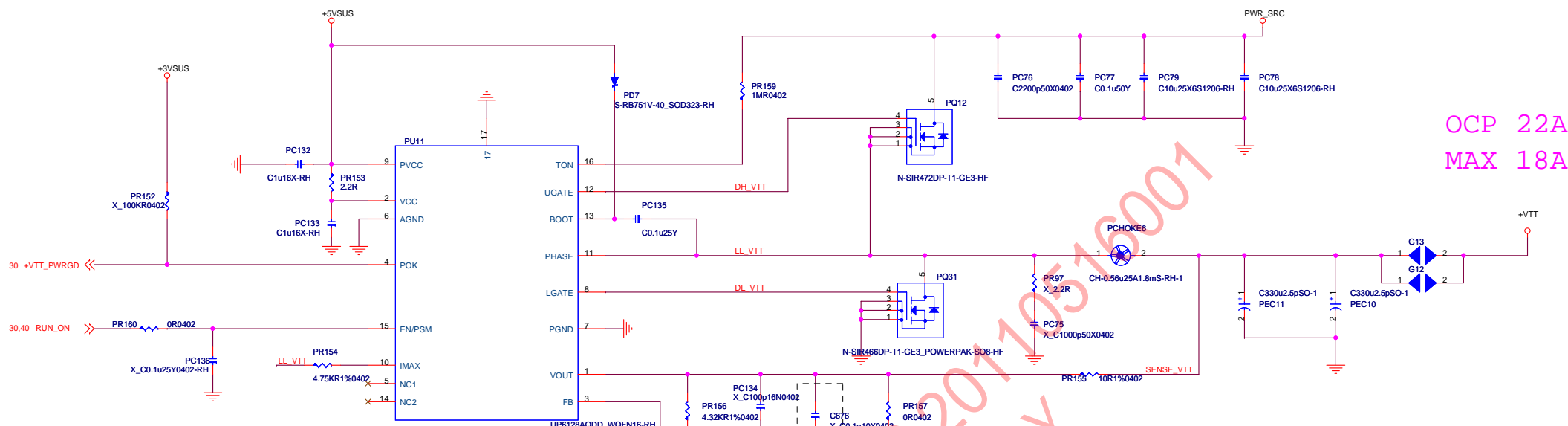
OCF 16A
MAX 12A

MAX 2A

8

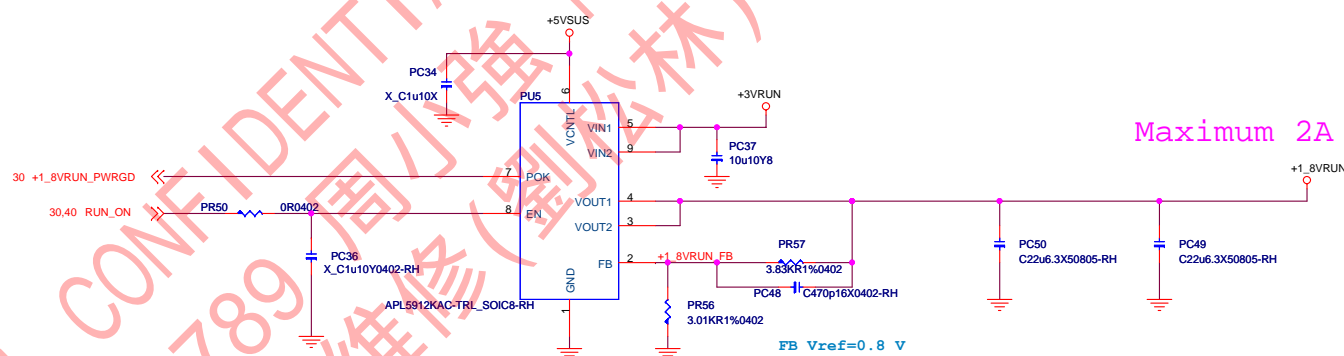
2

| MSI MICRO-STAR INT'L CO.,LTD. | | | |
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| SMDDR VTERM /1 5VRUN | | | |
| Size | Document Number | Rev | |
| Custom | MS-1688 | 0A | |
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OCF 22A
MAX 18A

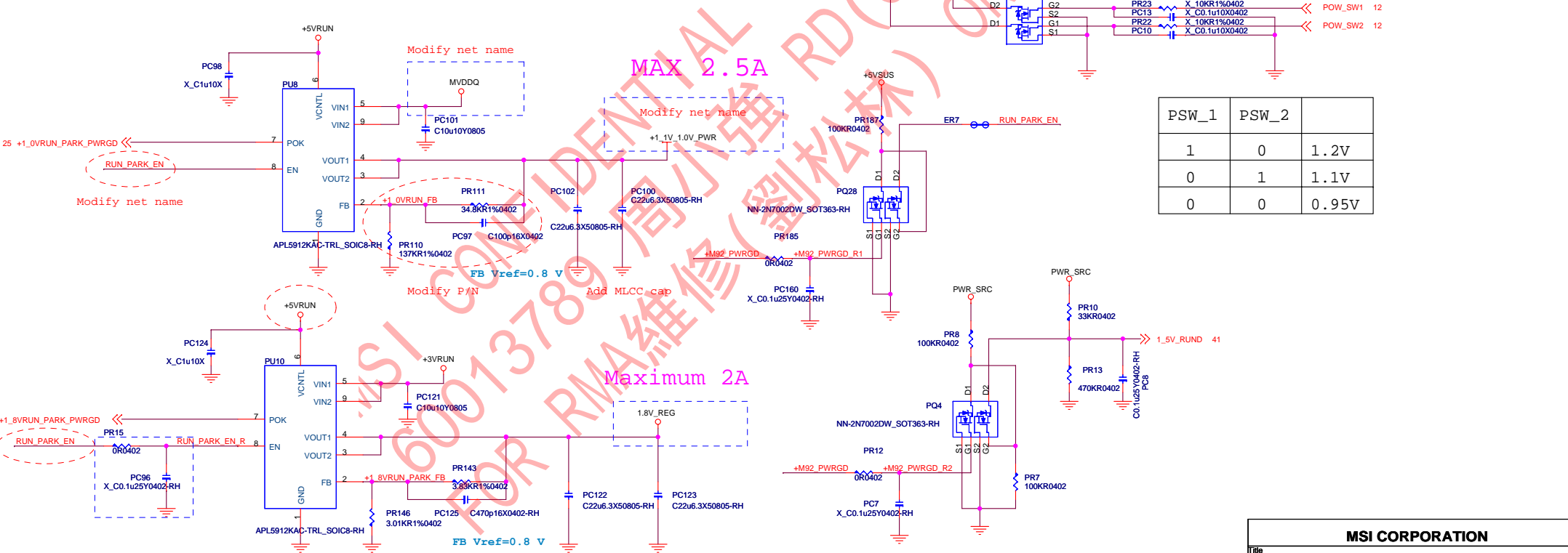
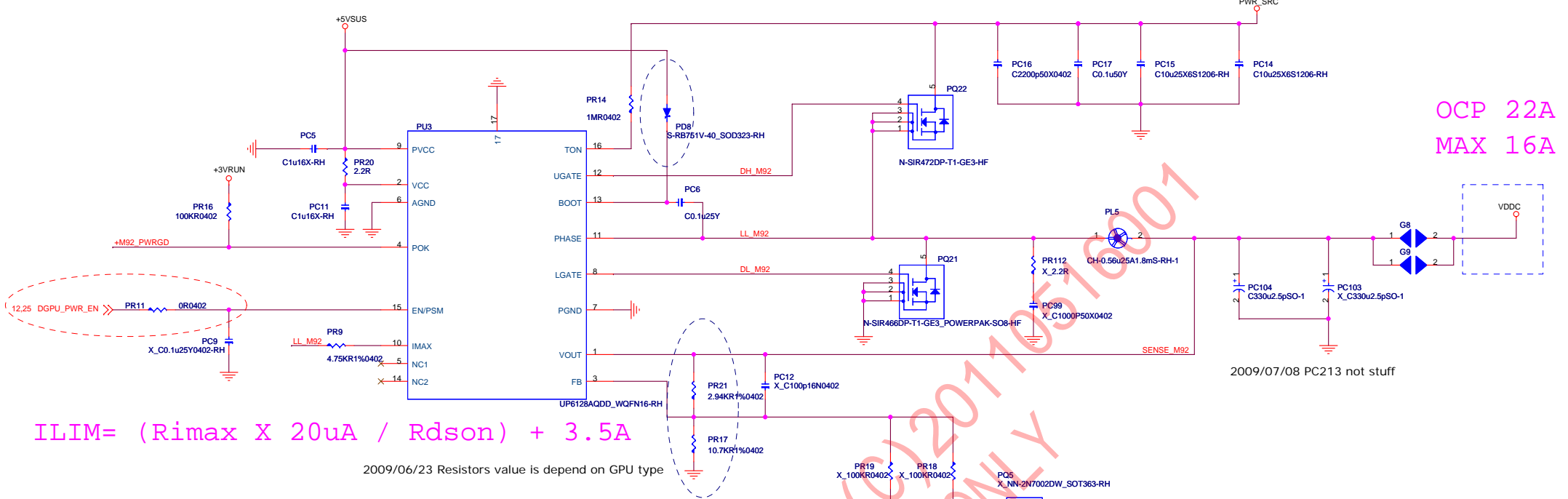
$$ILIM = (R_{imax} \times 20\mu A / R_{dson}) + 3.5A$$



Maximum 2A

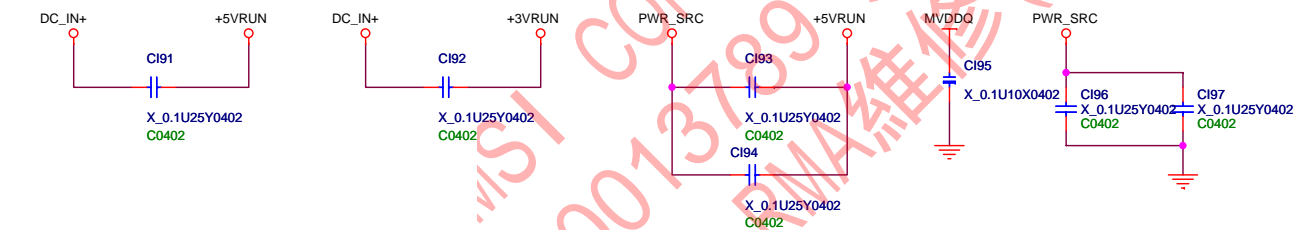
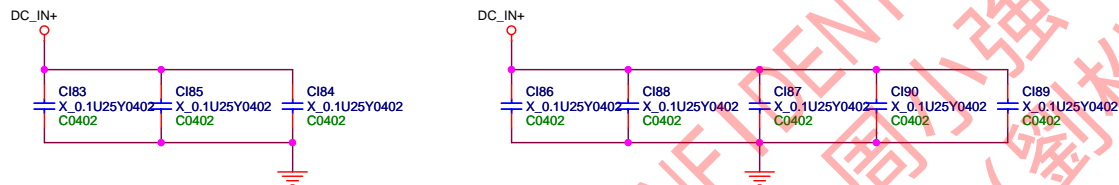
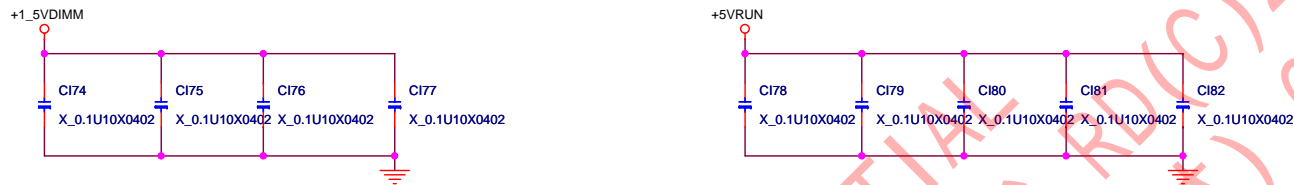
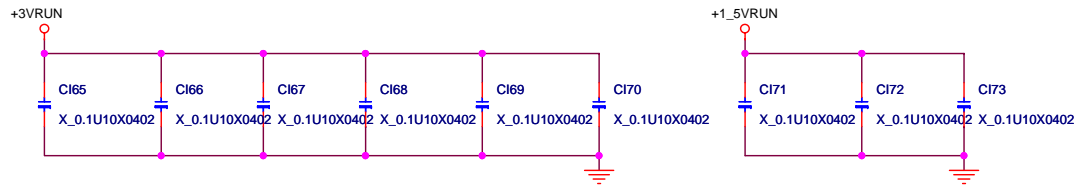
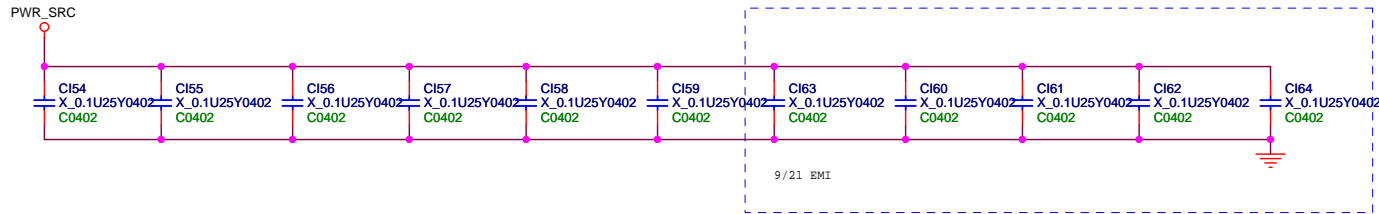
FB Vref=0.8 V


| MSI MICRO-STAR INT'L CO.,LTD. | | | |
|-------------------------------|---------------------------|-------|----------|
| Title | | | |
| VTT Power, +1.8VRUN | | | |
| Size | Document Number | Rev | |
| Custom | MS-1688 | 0A | |
| Date: | Tuesday, October 06, 2009 | Sheet | 42 of 52 |



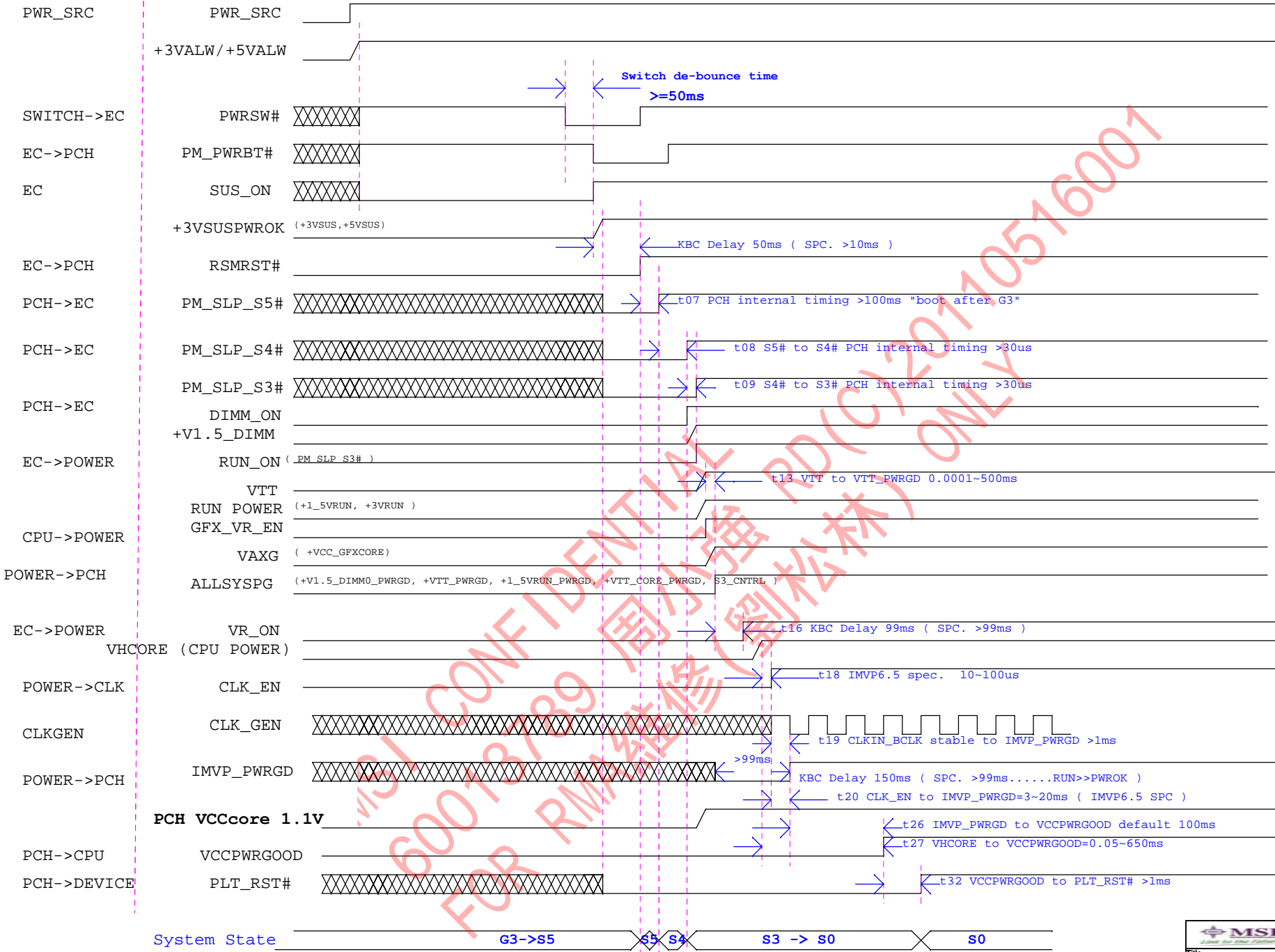
| PSW_1 | PSW_2 | |
|-------|-------|-------|
| 1 | 0 | 1.2V |
| 0 | 1 | 1.1V |
| 0 | 0 | 0.95V |

9/28 ATI suggestion:DPX_VDD10 should ramp up before DPX_VDD18



| | |
|--|-----------------|
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| EMI | |
| Size B | Document Number |
| MS-1688 | |
| Date: | Rev 0A |
| Tuesday, October 06, 2009 | Sheet 49 of 52 |

Calpella System Power on Sequence DC mode



Power down Sequence DC mode S0 to G3

